SECTION FOUR : CIRCUIT DESCRIPTION

4.1 SIGNAL CIRCUITS

The following should be read in conjunction with BP2219 1650/9 Receiver Block Diagram bound at rear. Refer to BP1978 1650/9 Chassis Interconnections and Misc. Modules for connections etc. between the modules described.

Circuit Diagrams BP2020 RF Board and 1st IF Board should be studied along with the following.

The input signal is passed via a 30MHz input low pass filter to a combined antenna mute and overvoltage protection circuit formed by 7RLA1,7D10 and 7IC1. The input signal is routed via a switchable 20dB aerial attenuator circuit (2 X 10dB sections) and switched by 7RLF1 to either the optional preselector circuit BP2088 or straight to a balanced RF amplifer 41TR2/3 (2 X BFW30). This amplifer has a flat response between 100kHz and 30MHz with additional negative feedback giving a gradual gain reduction down to 10kHz. The optional preselector is switched in when 'Wideband' is deselected.

Differential transformer outputs 41T2/3 from 41TR5/6 drive high level mixer 41IC1 (D6262) biased at 25mA i.e. 5V at 41TP4 adjusted with 41RV3. 'Up Conversion' provides an output at the 1st IF frequency of 46.205MHz which is filtered by 75ohm roofing filter 7FL1 at a bandwidth of 16kHz. /P receiver variants utilise a three port splitter/combiner 41IC3 (3306) to provide isolated low level IF output and drive to 7FL1. 41R16 and 41R18 compensate for impedance matching and insertion loss when 41IC3 is not fitted. The subsequent signal from roofing filter 7FL1 is applied to a double bridged 'T' attenuator 7D21-24 (4 X HP5082-3081) which provides up to 55dB of attenuation.

Attenuation control is performed by drawing current through i.e. turning 'ON' the shunt diodes 7D22,24 and turning 'OFF' the series diodes 7D21,23. This is performed by a voltage to current control circuit comprising 7IC7,7TR8,7TR9,7IC8,7TR10,7TR11 which enable attenuation control over the range 0-4.5V. CMOS op-amp 7IC7 (CA3140E) has RF AGC voltage applied via time constant components 7R31,7C35,7R34. Transistor 7TR7 (BC547B) is used to 'quench' the AGC voltage whenever AGC mode is changed or Sweep or Scan modes are in use. This allows AGC integration to start from zero whenever a new frequency is selected.

7TR12 (BFX89) provides gain and isolation between the AGC attenuator and the second high level mixer 7IC9 (D6262) biased at 18mA i.e. 7.5V at 7TP4. 'Down Conversion' provides an output at 1.4MHz where the signal is passed to the Main IF Audio Board (BP1976).

Both Mixer circuits 41IC1 and 7IC9 form part of the synthesiser - see Section 4.3 Synthesiser and VCO circuit.

The main selectivity of the receiver is provided at 1.4MHz by the Main IF Audio Board (BP1976) and this circuit should be studied along with the following.

The 1.4MHz signal from 7PL8 passes to one of seven selectivity positions, of which, six use crystal filters. Selection of the seven bandwidths is by BCD-decimal decoder 10IC1D (74LS145) selecting the relevant crystal filter 10FL1-6 for bandwidths 0.3kHz to 8kHz while 16kHz employs a 3dB matching pad 10R14-16. Diodes 10D1-7 protect the decoder outputs from extraneous voltages produced by relays 10RLA-H,10RLJ-N,10RLP. Each selectivity position uses relays on input and output to provide maximum isolation from each other, only the pair of relays associated with the chosen selectivity position is energised, the remainder being open circuit. The 16kHz position is effectively the bandwidth of the roofing filter 7FL1 on the 1st IF board. A 3dB pad matches the insertion loss of the other six selectivity positions and preserves the load impedance on the 2nd mixer circuit formed by 7IC9 and 7L2. 10C21 forms part of a capacitive attenuator with the O/C leakage capacity of 10RLN thus enhancing the isolation when the position is de-selected.

The 1.4MHz amplification is performed after the main selectivity. 10IC1,2 (MC1590G) and 10TR1 (BFR54) comprise a 90dB gain controlled amplifier some 80kHz wide. 10RV1 allows gain reduction matching between 10IC1 and 10IC2 under AGC conditions. 10TR1 is a high current high dynamic range buffer stage from where the signal is split off to the product detector and IF output stages.

Double balanced mixer 10IC7 (SL641) forms a product detector with 1.4MHz from the synthesiser board for SSB or CW detection while 10IC9 forms a combined AM and IF AGC detector.

Detector selection is by analogue multiplexer 10IC15 (MC14052B), the subsequent audio signal being amplified by 10TR7 (BC547B) and applied to 'low pass' filter 10C98,10CH4,10C99. 10IC18 (CA3240E)

forms a 'bandpass' active filter selected in CW mode by 10IC19 (14052B)

4.2 IF AGC CIRCUIT

IF AGC is derived from a fast acting AGC detector 10IC9 (SL623C). 10RV4 sets the point above which AGC output voltage is produced at 10TP8. 10IC15 (SL621C) produces audio derived AGC with mode and time constant being selected by 10IC5 (14052B). AGC selection is by two control bits via 10STC1 - AGC Mode LSB and AGC Mode USB. These AGC modes are described in Table 4.1.

Table 4.1
AGC Selection

MSB	LSB	Function	Time Constant
0	1	Audio Agc	Not Applicable
0	1	Man. Gain	Not Applicable
1	0	IF AGC	Short
1	1	IF AGC	Long

AGC voltage from 10D11 (BAX13) charges time constant capacitor 10C75 (22u) via 10R68 (2k2). 10R62 (100k) provides a discharge path for 10C75. This is the situation for 'FAST AGC'. Audio AGC time constant is provided by 10C92 (220u) at 10IC15-6 when audio AGC mode is selected. 10IC4a (CA3240E) provides a low impedance for level shifting by 10IC3b (CA3240E) and summing of 'AGC threshold' voltage from 10RV2 (2k2) by 10IC3a. 'Half rail' reference voltage is applied to both amplifiers (10IC3a,b) and any changes in it's level will not be seen at the output.

Variations in HT supply are not therefore superimposed onto the AGC control voltage output from 10IC3a.

RF AGC is developed completely separate from the 1.4MHz IF amplifier and is connected at all times. A two stage wideband amplifier 10TR8,9 drives a fast acting AGC detector 10IC12 (SL623C). RF AGC threshold is set by 10RV7 and the control voltage is routed to the 1st IF Board via 7PL5.

10IC6a (CA3240E) forms a mute comparator driven by 10IC6b, the AGC voltage and by 10IC4b, the IF gain control voltage. 10IC6a drives RLQ1 via 10TR3 (BC547B) providing external control while 10IC16 and 10IC17 provide audio muting by switching an

attenuator 10R85,86 into the audio signal path. 10TR4 and 22TR4 provide external indication for 'Carrier (Sideband) present'.

Two independently adjustable audio amplifiers are employed for line driving and external loudspeaker monitoring. The operation of the line amplifier is as follows. Junction FET 10TR11 (UC734B) drives the audio amplifier circuit 10IC20 (TBA810P) from a low impedance source, resulting in optimum low noise operating conditions for the latter. In order to maintain stability the bandwidth of 10IC20 is restricted by 10C141 (22n) and 10C142 (820p). The output is coupled via 10C149 (22u) and 10R131 (150R) to centre tapped line isolating transformer 10T1, allowing matching of a 600 ohm line to some 4 - 8 ohms for the amplifier. The transformer drives and terminates a 600 ohm line. 10IC21a acts as a half wave detector with 10D15 (BAX13) and with 10IC21b drives the 'line level' meter circuit on the display board via 11RS1-3. Operation of the external loudspeaker audio amplifier 10TR12 and 10IC22 is similar to the above. The output drives headphones via 10PL8 and 1SK8 and external loudspeaker via 10PL8 and 1SK4.

The Built In Test Equipment (BITE) system verifies the signal path by measuring the receiver's response to a wideband noise generator injected via 7RL1. 7TR2 (BC547B) is a reverse biased PN junction providing a 'white' noise source at a current set by 7RV1 (10k) and wide band amplified by 7TR3 (BFX89).

The Antenna Switch is operated by binary to 1 of 4 decoder 7IC4 (MC14555B) driving a buffer circuit 7IC5 (MC14050B). 7R26 (4 X 270R) provide current limiting on each output with decoupling by C27-30 (100n).

4.3 SYNTHESISER AND VCO CIRCUIT

The following should be read in conjunction with BP2158 1650/9 Receiver Synthesiser Circuits Block Diagram bound at rear. Refer to BP1978 1650/9 Chassis Interconnections & Misc. Modules for connections etc. between the modules described.

Table 4.2
Synthesiser Frequencies

Tuned Freq.	VCO Range	1st Loop	
0.010MHz	)	46.214MHz	
	) LF		
5.794MHz	)	51.998MHz	
	) LF+1		1st Oscillator is
12.794MHz	)	58.998MHz	46.204MHz above signal
	) HF-1		freq. in 2kHz steps.
20.794MHz	)	66.998MHz	
	) HF		
30MHz	)	76.204MHz	

2kHz step+	2nd Loop	Comparison Freq.	
0.005kHz	44.805,995MHz	5.995kHz	
			2nd Oscillator is
1.000kHz	44.805,000MHz	5.000kHz	1.4MHz below 1st IF
			in 5Hz steps
2.000kHz	44.804,000MHz	4.000kHz	

--oOo--

Example 4.1
19.999,995MHz Tune Frequency

19.999,995MHz Tune frequency is produced by 66.204,000MHz 1st oscillator & 44.804,005MHz 2nd oscillator.

Example 4.2
20.000,000MHz Tune Frequency

20.000,000MHz Tune frequency is produced by 66.204,000MHz 1st oscillator & 44.804,000MHz 2nd oscillator.

Example 4.3
20.000,005MHz Tune Frequency

20.000,005MHz Tune frequency is produced by 66.206,000MHz 1st oscillator & 44.805,995MHz 2nd oscillator.

Circuit diagrams BP2089 Synthesiser and VCO Board should be studied along with the following:-

The 1650/9 synthesiser is a two phase locked loop design. The first loop generating frequencies covering the tuned frequency range 10kHz to 30MHz in 2kHz steps, the second loop providing 2kHz interpolation in 5Hz steps. Table 4.2 shows the operating frequencies of the two loops, their setting and interelation being under software control. Worked examples are shown for particular tune frequencies in Example 4.1 to Example 4.3.

8IC2 (SP8690B), 8IC3 (LF356N), 8IC4 (HEF4750), 8IC5 (HEF4751) and 9TR1 (40673) form a phase locked loop circuit. 8IC4 functions as a dual output phase comparator, phase comparator 1 (PC1) is a sample and hold circuit providing a very accurate control voltage. Phase comparator 2 (PC2) is a wide range digital circuit with three states-positive, negative and high impedance. The output comprises a pulse train of varying mark/space ratio depending upon the phase difference between the reference (2kHz derived from the 5.6MHz standard) and the output of the variable ratio divider 8IC5. Close to lock PC2 becomes high impedance and sample and hold comparator PC1 takes over. This technique gives rapid switching and very low reference frequency sidebands. PC1 and PC2 are summed into a low noise integrator circuit 8IC3. The integrator is 'half rail' biased so that digital comparator PC2 may provide both positive and negative correction i.e. $\pm$ 6V. 'Out of lock' indicatior is available at 8IC4-1.

The variable ratio divider provides 2kHz output drive to the Phase Comparator. The divide ratio is set by 8D9-12 (BAX13), 8IC7 (MC14011B), 8IC8 (MC14504B) on a bit parallel digit serial basis. The variable ratio divider controls the 'divide by 10/11' prescaler 8IC2 which is driven by VCO buffer 9TR3 (40673).

The voltage controlled oscillator has four ranges, selected by relays 9RLA-D, in order to reduce the varicap diode control line sensitivity and the 'inband' phase noise. Separate buffered outputs are provided, 9TR2 (40673) for the 1st signal mixer and 9TR3 (40673) for the prescaler 8IC2.

The second phase locked loop generates frequencies in the range 44.804,000MHz to 44.805,995MHz in 5Hz steps which are applied to the second signal mixer.

8TR7 (BFX89), 8XTL1 (14935kHz) and 8D16 (MV1648) form a third overtone voltage controlled crystal oscillator (VCXO). 8TR6 (40673) amplifies and splits the oscillator signal, from the drain via 8PL9 to the 2nd signal mixer and from the source, tapped down by 8RV5 (220R), to IC26 (SL1641). Mixed with the eighth harmonic of 5.6MHz it produces an output in the range 4kHz to 5.995kHz. 8IC28 (MC14001B) acts as an amplifier/limiter to produce a 15Vpp squarewave to feed phase comparator A input of 8IC27 (MC14046B). 8IC31 (MC14526B) and 8IC32 (MC14569B) form a variable ratio divider preset by two eight stage shift registers 8IC33,34 (MC14094B). The output from the variable ratio divider is in the range 4kHz to 5.995kHz and is fed to phase comparator B input 8IC27 via 8IC28 (MC14001B). 8IC25 (CA3240E) amplifies the phase comparator error voltage produced and applies it to varicap diode 8D16 (MV1648). Altering the variable ratio divider under software control pulls the VCXO over it's 2kHz range. 'Out of lock' detection is provided by 8IC29, 8D17 (BAX13), 8R73 (100k) and 8C110 (10n). The output at collector 8TR9 (BC547B) is 'ORed' with the first phase locked loop 'out of lock' detector at 8STC1-1 where it's state may be read by the micro-computer.

The 5.6MHz standard is 8OSC1, a voltage controlled ovened crystal oscillator. Trimming is via 8RV2 (1k) and the signal is shaped and distributed to the two phase locked loops and BFO circuit via 8IC15 (74LS04).

The beat frequency oscillator (BFO) employs a single phase locked loop circuit with a centre frequency of 1400kHz tunable in 100Hz steps over the range $\pm$ 3.9kHz under software control. Mosfet 8TR4 (40673)

forms a tuned gate oscillator with 8L1,C57,C56 which is varactor diode controlled by 8D15 (MVAM115). The oscillator is buffered by 8TR3 (BFR54). Quad NAND gate 8IC19 (MC14011B) acts as an amplifier/limiter feeding 15Vpp square wave to variable ratio divider 8IC23 (MC14569B) and 8IC22 (MC14526B). The resulting 100Hz signal is applied to the A input of the phase detector 8IC21 (MC14568B). Programmable divider 8IC18 (MC14569B) divides the output from the 5.6Mhz standard 80SC1 by 140 and dual 'D' type bistable 8IC20 (MC14013B) further divides by 4 to produce 10kHz at 8TP6. An internal divide by 100 in 8IC21 produces a 100Hz signal which is applied to the reference B input of the integral phase detector. Error voltage is applied to the varactor diode 8D15 via 8R38 (1M) and lag-lead filter 8C61 (1u) and 8R39 (39k). 8TR5 (BC547B) signals 'Out of Lock' to the micro-computer via 8STC1. The oscillator output at 8IC19-11 is filtered by 1400kHz parallel tuned circuit 8CH3 (33uH), 8C45 (330p) and output to the product detector via 8PL7.

In SSB mode the BFO phase locked loop is disabled by a low '0' on dual NAND gate input 8IC19-13 while dual 'D' type bistable 8IC17 (MC14013B) configured as a divide by 4 circuit is enabled to provide 1400kHz from the 5.6MHz standard 80SC1. The signal is passed via 8R26 (10k) and 8C47 (10n) to the previously described 1400kHz parallel tuned circuit.

4.4 EXT. STANDARD ADAPTOR BOARD suffix /S receivers

Circuit Diagrams BP1712 External Standard Adaptor Board and BP2089 Synthesiser and VCO Board should be studied along with the following.

The External Standard Adaptor circuit phase locks the 5.6MHz ovened crystal oscillator to an external signal of either 5MHz or 1MHz.

The external standard input at 17P11 is taken via 50 ohm 10dB pad to wideband gain controlled amplifier 17IC6 (SL1610) with 17TR1 (BCY71) acting as AGC detector. 17IC7 (741) acts as a threshold detector driven from the AGC input of 17IC6, switching relay 17RLA1 at the appropriate level. 17IC4 (MC14001B) amplifies and limits the 'external standard' signal to 15Vpp and drives variable ratio divider 17IC5 (MC14569B). The scale factor may be set to either divide by 10 or 50 depending upon links 5 and 6. The 5.6MHz ovened crystal oscillator signal from the synthesiser board via 17SK1 is divided by 56 by 17IC1 (MC14569B). 17IC2a (1/2 MC14001B) comprises a 'pulse stretching' circuit with D1,R2 and C3. Phase comparator 17IC3 (HEF4046B) compares the 5.6MHz crystal oscillator and external standard frequencies at 100kHz and produces a correction voltage at 17TP2 which is fed back to the varactor control input of the internal ovened crystal oscillator via RLA1 and 17SK2. 17RLA1 only switches the 5.6MHz ovened crystal oscillator varactor control input over when there is sufficient level of external standard, otherwise the control voltage is provided from a reference voltage on the synthesiser board. 17IC2b (1/2 MC14001B), D2, R8, C14 and C15 form an 'out of lock' detector via 17TR3 (BC547B) while 17TR2 (BC547B) detects the external standard level - both of these functions being output to the microcomputer via 17PL2.

4.5 NBFM BOARD suffix /N receivers

Circuit Diagrams BP1977 NBFM Board and BP1976 Main IF Audio Board should be studied along with the following.

Narrow band frequency modulation detection utilises a down conversation technique from 1.4MHz to 455kHz.

40IC1 (MC3359) comprises a six stage limiting IF amplifier with integral Colpitts oscillator and double balanced mixer. L2,C21 form the quadrature FM detector tuned circuit with recovered audio being output at 40PL2-6. An active filter comprising 40R12,40C19 and 40C20 produces a noise band which drives noise detector 40D1 (BAX13). 40RV1 provides

noise detector threshold adjustment with the mute signal output at 40TP3. 40IC3a (1/2 CA3240E) forms a comparator with 'hysteresis' to produce the mute signal (inverted) at 40PL2-5 while 40IC3b provides level shifting of the AFC output so that it may drive the meter circuit via 40PL2-7. Dual gate MOSFET TR1 (40673) forms an RF switch to enable the NBFM circuit 40IC1. Some 40dB of attenuation is provided in the 'off' position - gate two at zero volts, so minimising any interference that may be caused by the NBFM circuit in other modes. Diode 40D2 (BAX13) discharges 40C30 (1u) so that the mute signal from 40IC1-15 is always integrated from zero each time the NBFM circuit is selected i.e. during 'scanning'.

4.6 FSK DETECTOR BOARD suffix /K receivers

Circuit Diagrams BP2162 FSK Detector Board and BP1976 Main IF and Audio Board should be studied along with the following.

The Frequency Shift Keying Detector provides an output of ±10V centred on 1.7kHz for frequency shifts of ±45Hz to ±500Hz.

42TR1 (BC547B) buffers and low-pass filters the 1.7kHz signal from 42PL1-6 which is amplified and limited by 42IC1 (MC1590G) to some 700mVpp. This output is split off into two paths, one via 42C24 (10u) to the 'osc' input of high level mixer 42IC4 and the other to bandpass filter 42IC2a and phase shifting circuit 42IC2b. 42IC2a (1/2 CA3240E), 42C10,11 and 42R10 form a bandpass active filter with 45° (-3dB) points at ±410Hz from 1.7kHz while 42RV1 (2k) provides for centre frequency adjustment. CR network 42C12 (10n) and 42R17 (10k) driven by unity gain inverting amplifier 42IC2b (1/2 CA3240E) produces a 90° phase shifted signal at 42IC3-3 (CA3140E). 42IC3 provides a high impedance for the 90° phase shifting network. Double balanced mixer 42IC4 (SL6440) acts as a detector providing two out of phase outputs at 42TP2 and 42TP3 centred about 6.6V for 1.7kHz input while 42RV3 (100R), 42R27,28 (470R) allow DC balancing of the outputs. The identical low pass filters following ensure that any waveform distortion introduced will be balanced out by dual comparator circuit 42IC7 (LM339). This circuit amplifies and limits the out of phase signals and by introducing equal amounts of hysteresis to both waveform edges so cancels the distorting effects already mentioned. 42IC9 (MAX232) converts the 5V (>1.7kHz) or 0V (<1.7kHz) signal to -10V or +10V with respect to ground (RS232C). 42TR2,TR3 (BC547B) allow the FSK Detector to be deselected by forcing one of the outputs of the

detector 42IC4 low and so holding the output at 42PL2 at either minus or plus 10V. Either idle state may be selected by changeover switch 42SW1. 42R33 (47k) and 42C37 (10u) integrate the FSK signal from comparator 42IC7a and with 42IC6 (CA3140E) provide a drive signal for the centre zero meter circuit via 42PL1.

4.7 CONTROL, DISPLAY AND MICRO-COMPUTER CIRCUITS

The following should be read in conjunction with BP2159 1650/9 Receiver, Control and MCU Circuit, Circuit Diagram BP1992 1650/9 Interface Board, BP1996 1650/9 Front Panel Display and BP1953 1650/9 16K Micro-Computer Board bound at rear. A simplified program executive flowchart BP2220 should also be studied.

The micro-computer unit uses a MC6809P microprocessor (MPU 13IC12), 16K bytes of 'read only memory' (ROM-2 X 27C64, 13IC8,9), 2K bytes of 'random access memory' (RAM-TC5517APL, 13IC5), and programmable timer module 13IC1 (MC6840P). Eight external peripherals may be accessed by the system. All of the RAM is non-volatile, it's power being supplied by a 3.6V 100mAH battery when the receiver is 'off'. Circuitry is incorporated in order to prevent memory corruption at power down during a 'write' to RAM. 13IC7-4,5,6-8,9,10 (74HC00) form an RS bistable. At power down the RS bistable changes state because current is no longer supplied to opto-isolator 13IC15 (MCT2), in doing so the 'chip select' pulse to 13IC5 (TC5517APL) is inhibited. If, however, a power down occurs during a 'write ' period this is completed as 13IC7-6 cannot change state when it is low (0). The RAM is therefore never deselected during a 'write' period. Threshold comparator 13IC6 (CA3140E) detects the supply falling to approx. 8.3V (from 10V) and disables opto-isolator 13IC15. 0.5V hysteresis is incorporated around the switch over point to prevent mis-triggering. 13IC4 (MC14528B) forms a monostable with 13R16 (100k) and 13C13 (10u) which generates a reset pulse (100-200mS) at power up and from 13IC15-4 going momentarily low (0). This reset pulse is coupled to 13IC12 via 13TR1 (BC547B) allowing the MPU reset vectors to be loaded.

All data lines and address lines A0-A11 are 'pulled up' by 13R2 (47k) and 13R41, 13R20-22 (47k) in order to provide known states during power down. Partial decoding is used by the MPU to address both on and off board peripherals. The repeats that occur are not accessed by the software.

It is important that data remains static on the data bus D0-D7 (13IC12-24-31)for at least 30nS after the enable line (13IC12-34) goes low (0). In order to improve the margin of safety all peripherals are enabled via leading edge triggered monostable 13IC11 (74LS123). The resulting 'output enable' is shorter, approx. 450nS as opposed to the 'input enable' of 610nS. This gives a much greater margin of safety i.e. 610-450=160nS before the 'input enable' falls

but with the data lines being static until at least that time. The actual monostable time is not critical to the system operation. The delay provided removes any possible race hazard between enable and data caused by 'clock skewing'.

13IC1 (MC6840P) is a programmable timer module used to control the optional preselector BP2088 as well as read the output from the control knob and generate the 'warble tone' from the piezo sounder 11PZ1. 13IC1 (MC6840P) comprises three 16 bit binary counters, three corresponding control registers and a status register. The programmable timer module is used by the micro computer whenever the control time is going to be long compared with the MPU cycle time i.e. operating the preselector motor or the piezo sounder. This allows the micro-computer to continue operation while the timer takes over these tasks, so avoiding any possible control 'lock out' situation arising.

The micro-computer sends and receives mainly serial data signals to and from the receiver via the interface board BP1992. The LED front panel display is controlled by octal D type latch 12IC17 (74HCT374) at peripheral address $2005. Data is converted to latched parallel form by display drivers 11IC4,5,6,7 (4 X MM5450). Data is latched into the display driver after 35 serial data bits have been sent. The LED front panel display is fully static in operation. The synthesiser (see Sect 4.3 Synthesiser and VCO circuit) is controlled by octal D type latch 12IC7 (74HCT374) at peripheral address $2004. 12IC2,3 (MC14094) form a 16 stage shift register which converts a serial data, clock and strobe signal (TP2,3,1) into 16 static outputs controlling AGC mode, bandwidth and mute through to AGC quench and aerial attenuator.

Analog functions within the receiver i.e. IF gain control, carrier operated relay etc. are interfaced to the micro-computer by 8 bit successive approximation A-D converter 12IC10 (ZN439E) and 6 bit D-A converter 12IC12 (ZN436E). The A-D converter 12IC10 is connected directly to the data bus and is located at peripheral address $2001. 12IC9 (7555) generates a negative line for 12IC10 with voltage doubler circuit 12C14,15 and 12D4,5. 12RLA1 allows either the IF gain control voltage to be read in 'local' operation or the meter voltage to be read in 'remote'. 12RV1 (50k) provides full scale adjustment for A-D converter 12IC10 which operates in continuous conversion mode, independently of the micro-computer, with a clock frequency of approx. 50kHz. The D-A converter 12IC12 (ZN436E) comprises an R-2R ladder network and is buffered from the data

bus by octal D type latch 12IC13 (74HCT374). The D-A converter output is scaled by 12IC11 (CA3140E) and 12RV2,3 (20k) and provides IF gain control voltage at 12TP5 in 64 discrete steps over the range 1.25-4V approx.

All the front panel keys, with the exception of 'STANDBY' are organised as a six by six matrix. In order to reduce radiated interference, this matrix is only 'actively' scanned on demand. Key board 'write' signals from 12IC16 (74HCT374) go to the six keyboard matrix rows. The six keyboard matrix columns are 'read' by 12IC15 (MC14503B) and 'pulled up' by 12R31 (2k2). Normally all the rows are held low (0) and, with no key pressed, all the columns are high (1). The keyboard is read in this fashion every 50mS. A key press causes one of the columns to go low (0) and this initiates a scan routine by the micro-computer. Each row in turn D0-D5 (12IC15) and D7 (12IC6) is taken low (0) and the corresponding column is identified by 12IC15. A consecutive scan, 50mS later, will cause the micro-computer to act on the key press, however any change will cause the key press to be ignored and a return to the normal reading routine.

The tuning knob provides two inputs to the programmable timer module 13IC1 (MC6840P) via 11IC1 (MC14583B), 11IC2 (MC14077B) and 11IC3 (MC14C06B). These circuits convert the two-phase pulse stream from the turned knob into separate 'Up' (knob turning clockwise) and 'Down' (knob turning anti-clockwise) pulse streams which can be separately counted and accumulated by the micro-computer.

SECTION FIVE : MAINTENANCE

WARNING

⚠ When working on the Receiver it may be necessary for power to be applied. In this circumstance normal precautions for safety MUST be observed. Attention must, in particular, be paid to the voltages present at the supply fuse and the mains transformer located under a protection cover at the rear of the receiver. The protection cover should remain fitted at all times.

5.1 ALIGNMENT AND FAULT FINDING

The Receiver is suitable for continuous use under arduous conditions and normally requires no routine maintenance. Re-alignment should only be attemped in absolute necessity and with suitable test equipment and tools. The Receiver is generally tested and aligned in it's completely assembled state. However, the VCO and front panel assemblies may be more conveniently tested when removed from the receiver and powered from the appropriate 'test boxes'. Reference is made throughout the maintenance section to the use of 'test boxes'. These considerably facilitate the testing of circuit boards and the interfacing of test equipment to the Receiver. Test box circuit diagrams are provided bound at rear while complete units may be purchased from Eddystone Radio quoting the relevant part numbers.

5.1.1 ALIGNMENT OF SYNTHESISER AND VCO

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Digital Frequency Meter with low capacity input.

4) Distortion Factor Meter with 600ohm termination.

Procedure:-

Note the position of all wiring and the position of earth straps on a particular Receiver.

1) Check the outputs of all voltage regulators

8IC1 = +5V
8IC6 = +12V
8IC12 = +5V
8IC13 = +12V
8IC14 = +12V

} ± 5%

2) Connect digital voltmeter to link pins 5 and 6 (near 8PL4) and adjust multi-turn pot 8RV2 for +3.5Vdc.

3) Connect oscilloscope to 8IC15-1 and check that 5.6MHz oscillator output is approx. 5Vpp. Use a digital frequency meter to determine frequency of 5.6MHz crystal oscillator, adjusting trimmer in 8OSC1, if necessary, with an insulated trimming tool. Accurate alignment is best carried out on a complete receiver and is detailed in Section 5.1.?.

Second Loop Alignment

4) Connect oscilloscope to junction 8D16 and 8R60 and check 14.935MHz oscillator is approx. 4-6Vpp.

5) Connect oscilloscope to 8PL7-1 and adjust 8RV3 for 300mVpp.

6) Tune Receiver to 1001.000kHz.

7) Adjust trimmer 8C100 to mid-capacity. Connect oscilloscope to 8TP11 and peak trimmers 8C73 and 8C95 for maximum output.

8) Adjust 8RV5 for 500mVpp at 8TP11.

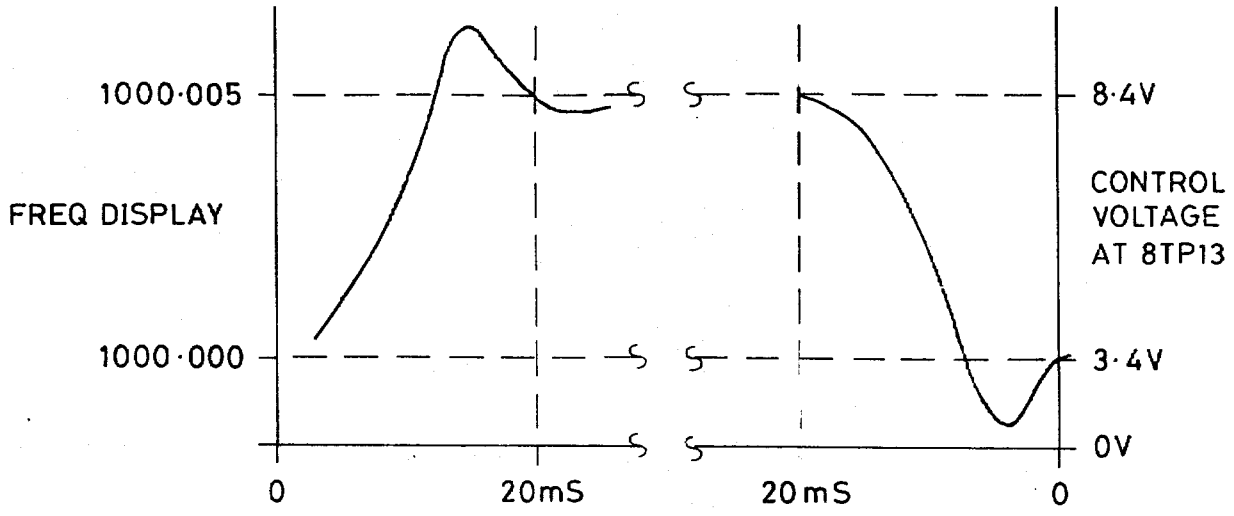
9) Connect digital voltmeter to 8TP13 and adjust trimmer 8C100 for 5.6Vdc

10) Iteratively peak 8C73, 8C95 and set 8C100 until interaction ceases.

11) Tune Receiver to 1000.005kHz and check voltage at 8TP13 is approx. +8.3Vdc. Tune Receiver to 1000.000kHz and check voltage is +3.5Vdc approx.

N.B. Tuning between these two frequencies produces the switch waveform in Figure 5.1.

Figure 5.1
Dynamic response of second loop synthesiser for a 2kHz step.



12) Monitor 7TP11 (RF/1st IF PCB 7) via low capacity probe and good RF earth and peak 8C85. Set 8RV4 for 300mVpp. Note that signal at 7TP11 does not vary in amplitude when Receiver is tuned from 1000.005kHz to 1002.000kHz.

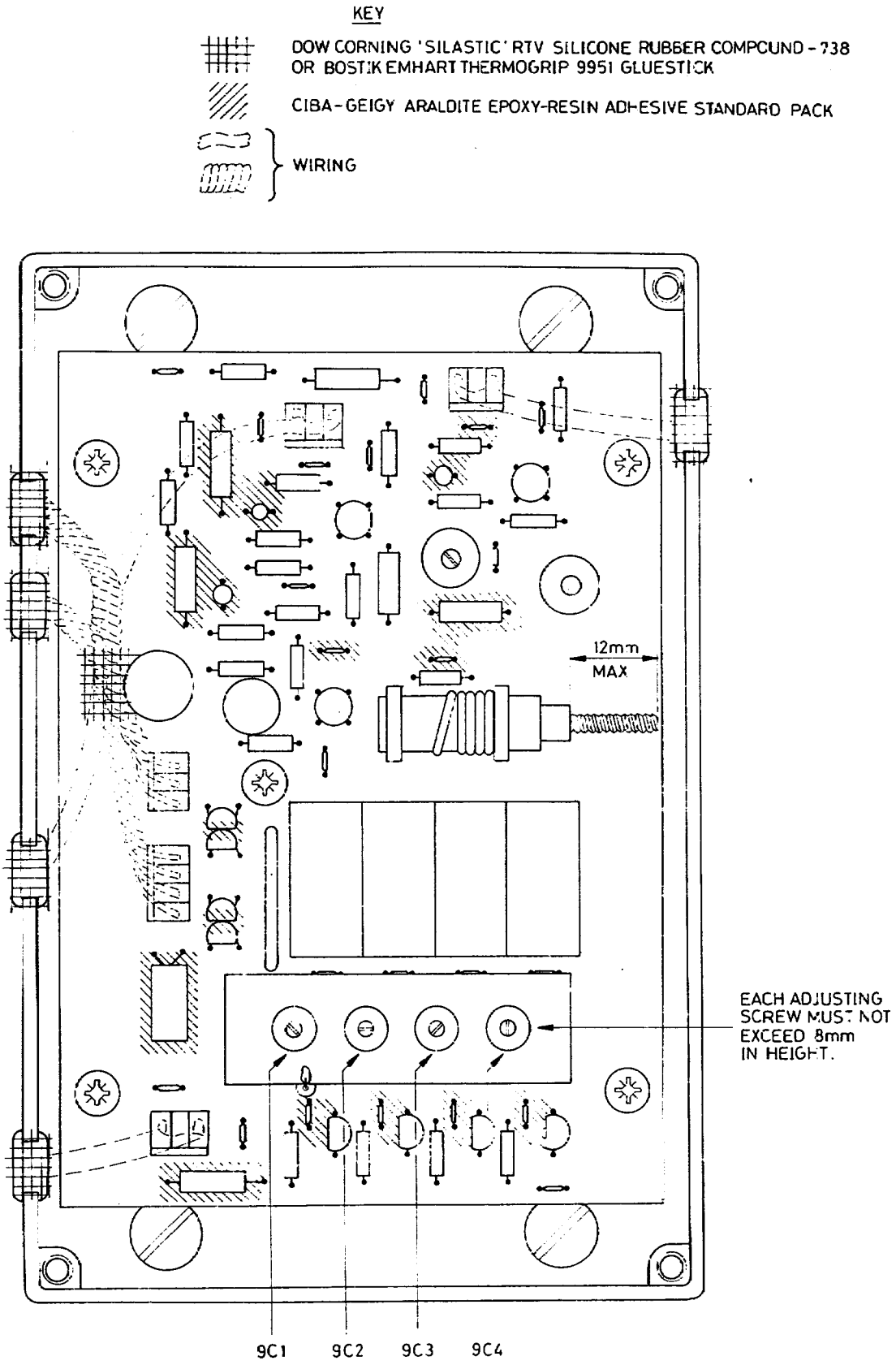
First Loop Alignment

13) Set 8RV1 1/3rd of a turn from fully anti-clockwise and ensure that 8IC3-7 is approx. +14.5Vdc. 8RV1 affects the 'lock-in time' of the First Loop.

14) Monitor 8TP2 (divice by 10/11 prescaler I/P) via low capacity probe and good RF earth and check that the signal level is typically 400-800mVpp when Receiver is tuned over the range 10kHz to 30MHz.

15) Check that the waveform at 7TP4 (RF/1st IF PCB 7) via low capacity probe and good RF earth is reasonably sinusoidal and at least 400mVpp at 29MHz.

Figure 5.2
VCO Board Details



16) Tune Receiver to 5.793,995MHz and monitor dc voltage at 8PL1. Adjust to 11.5V with trimmer 9C4 in VCO box as detailed in Figure 5.2. Tune Receiver to 5.794,000MHz and note dc voltage falls to between +3.5V to +5.5V.

17) Tune Receiver to 12.793,995MHz and monitor dc voltage at 8PL1. Adjust to 11.5V with trimmer 9C3 in VCO box as detailed in Figure 5.2. Tune Receiver to 12.794,000MHz and note dc voltage falls to between +3.5V to +5.5V.

18) Tune Receiver to 20.793,995MHz and monitor dc voltage at 8PL1. Adjust to 11.5V with trimmer 9C2 in VCO box as detailed in Figure 5.2. Tune Receiver to 20.794,000MHz and note dc voltage falls to between +3.5V to +5.5V.

19) Tune Receiver to 29.999,990MHz and monitor dc voltage at 8PL1. Adjust to 11.5V with trimmer 9C1 in VCO box as detailed in Figure 5.2. Tune Receiver to 10kHz and note dc voltage falls to between +3.5V to +5.5V.

N.B. No trimmer screw should protude by more than 8mm. If this occurs retune the lowest frequency range, adjusting the tune of 9L1 to allow more capacity. Coil 9L1 should have approx. 12mm of clear thread, after adjustment repeat steps 16-19.

BFO Alignment

20) Select SSB mode and connect oscilloscope to 10TP6 (BP1976 Main IF and Audio Board). Adjust 8RV3 for 300mVpp.

21) Select CW mode and set BFO to 0.0kHz. Adjust 8L1 fully anti-clockwise and observe the BITE LED flashing.

22) Connect a digital voltmeter to 8TP7 and adjust 8L1 for +2.5Vdc. Confirm that the BITE LED is extinguished.

23) Connect digital frequency meter to 10TP6 and digital voltmeter to 8TP7. Set BFO as Table 5.1 and verify performance at the test points concerned.

Table 5.1
BFO Control Voltages

BFO	10TP6	8TP7
+3.9kHz	1396.1kHz	2.8Vdc
0.0kHz	1400.0kHz	2.5Vdc
-3.9kHz	1403.9kHz	2.25Vdc

24) Check BFO signal is present at 10TP6 (300mVpp) when FM mode is selected.

N.B. BFO stability is affected by the value of 8R34 (nominally 470R). Where parts associated with the oscillator have been replaced i.e. 8TR4,8L1 etc. then slight adjustment to the value may be necessary in order to improve the CW Sinad measurement.

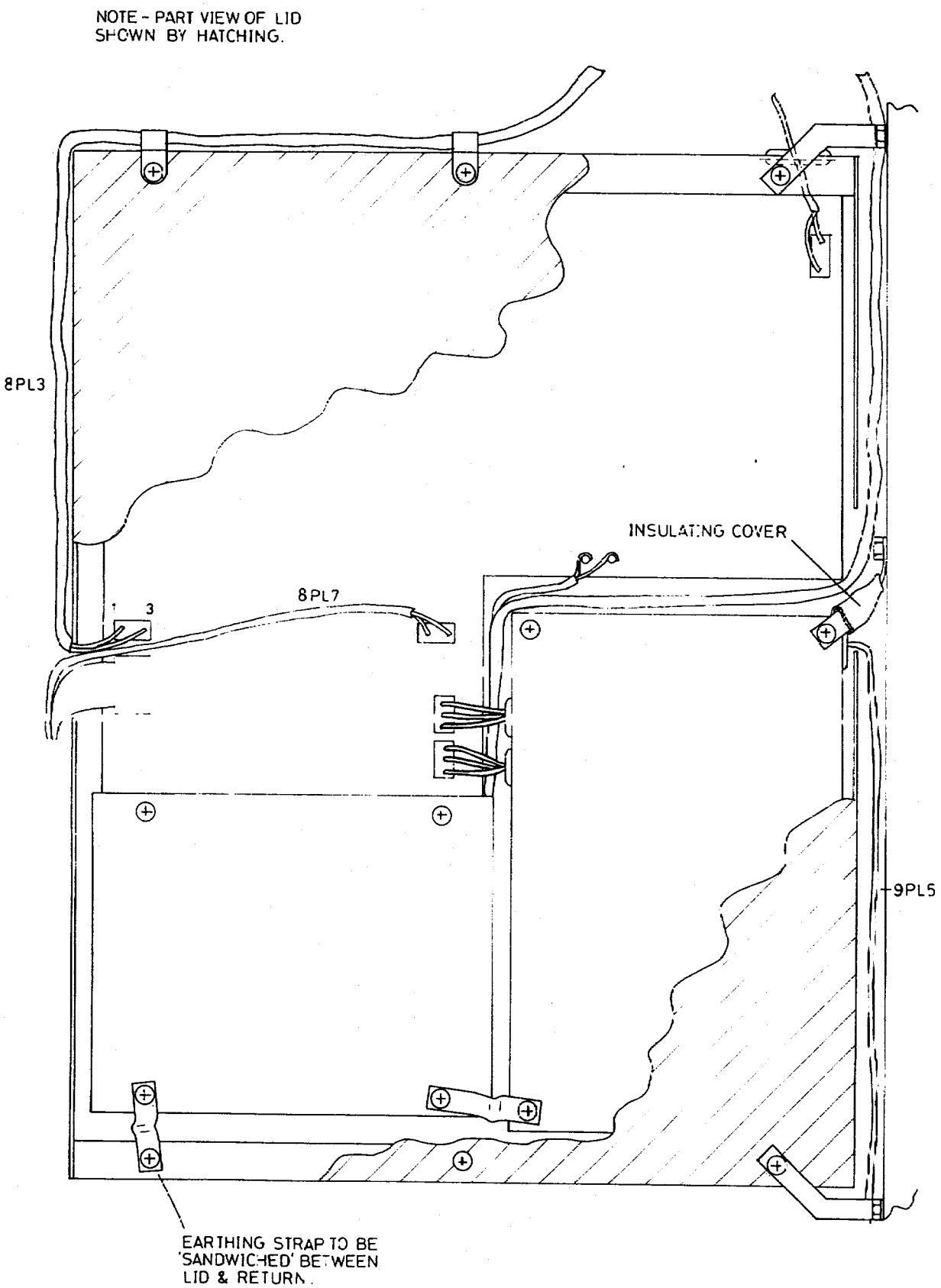
'Out of lock' Indication

25) Adjust 8RV5 for negligible signal at 8TP11 and observe the BITE LED flashing. Restore 8TP11 to 500mVpp with Receiver tuned to 1001.000kHz.

26) Disconnect 8PL2 and observe the BITE LED flashing.

27) Reconnect 8PL2 and observe the BITE LED extinguished. Replace earth straps and position wiring and check by listening on a distortion factor meter for any extraneous backround noise. See Figure 5.3.

Figure 5.3
Earth Strap/Wiring Position in Synthesiser Box



5.1.2 ALIGNMENT OF VCO BOARD

Where a VCO board has been repaired or a replacement is to be fitted it is advisable to initially align the circuit by itself as follows:-

Equipment required:-

1) Digital Voltmeter.

2) VCO Test Box D6248

3) VHF Oscilloscope with 50ohm inputs to load both VCO outputs simultaneously.

4) Digital Frequency Meter (100MHz) with low capacity input.

Procedure

1) Install the VCO board into VCO Test Box D6248 and connect to +15.5V regulated supply. Connect a digital frequency meter to the o/p socket. Select VCO range 'LF'.

2) If a new coil has been fitted set the output frequency to 46.2MHz (±50kHz) with +4.5V at 9PL1 by adjusting the coil winding of 9L1 (the screw adjuster should remain at approx. 12mm of clear thread).

3) Set the output frequency to 52MHz (±50kHz), with +11.5V at 9PL1, using 9C4.

4) Iterate 2 and 3 until satisfactory. (Note it is allowable if 46.2MHz is obtainable with the control voltage in the range +3.5V to +5.5V, especially if other VCO ranges do not align correctly or in the case where a coil is already 'araldited').

5) The remaining three ranges should be selected in turn and the HF end set with the appropriate trimmer (control voltage at +11.5V). The LF ends should then be obtainable within the control voltage range +3.5V to +5.5V. (See Section 5.1.1. for frequencies).

N.B. No trimmer screw should protrude by more than 8mm, if this occurs check the adjustment of the LF range.

6) Check the output level at 9PL4 and 9PL5, peaking these at 76.2MHz, with 9C5 and 9C6. These trimmers interact and the equalisation and peaking is best carried out by observing each output, terminated in

50ohm, simultaneously on a double beam oscilloscope. (With correct adjustment both trimmers should be close to minimum capacity).

7) Check coil assembly and components around the varactor diode are fixed with 'twin pack slow setting ARALDITE' to prevent movement under vibration. See Figure 5.2.

5.1.3 ALIGNMENT OF MAIN IF/AUDIO BOARD

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Digital Frequency Meter with low capacity input.

4) Distortion Factor Meter with 600ohm termination.

5) Audio Power Meter (4-8ohm).

6) Ancillaries Test Box D6447.

7) 1.4MHz IF Pad D6249.

8) Sensitive RF millivoltmeter.

9) 50ohm load.

10) Signal Generator 10kHz - 110MHz/50ohm.

Procedure :-

1) Connect the distortion factor meter and the audio power meter via the ancillaries test box D6447 to the ancillaries connector 1SK4.

2) Select AGC off, SSB mode, USB bandwidth, MUTE off and REMOTE off.

3) Set 10RV1 central, 10RV2 fully anticlockwise 10RV5 fully clockwise and 10RV6 fully anti-clockwise.

4) Check IF GAIN voltage range at link 2-3 is 1.25V with IF GAIN control fully clockwise and 4.0V with IF GAIN control fully anti-clockwise.

If necessary, adjust front-panel potentiometers 12RV2 and 12RV3 to achieve this.

5) Connect oscilloscope to 10TP6 and measure 1.4MHz

carrier insertion oscillator. Adjust 8RV3 on synthesiser board to give 300mVpp.

6) Adjust IF GAIN control for 2 volts at link 2-3.

7) Connect oscilloscope to 10TP4 and signal generator set at 1399kHz with 1.4MHz IF Pad D6249 to 10PL1. Adjust generator o/p to produce an indication on the distortion factor meter (1kHz tone). Tune L1,L2 and L3 for maximum AF output, reducing generator o/p to prevent overloading of the IF.

Note level required to produce 500mVpp on oscilloscope (typically 34uVemf). Adjust line level potentiometer 11RV2 for 1mW (0dBm) on distortion factor meter.

IF AGC Adjustment

8) Adjust 10RV2 for 1dB reduction in output on distortion factor meter. Increase the generator o/p by 1dB, to restore original output (this is the IF AGC threshold level). Connect DVM to 10TP8 and adjust 10RV4 for 2V. Measure SINAD (20-25 dB).

9) Set IF GAIN fully anti-clockwise and increase the generator level to restore 500mVpp at 10TP4. This should be 60dB>threshold level. If <60dB, re-adjust IF GAIN range to 1.25V and 4.1V (see (4) above).

10) Select 16kHz bandwidth, set generator to threshold level and frequency to 1.4MHz. Adjust IF GAIN control for 2V at link 2-3.

11) Connect the IF o/p 1SK6, terminated in 50 ohms, to the oscilloscope. Check o/p is approx. 50mVpp.

12) Connect a sensitive RF millivoltmeter to the IF o/p 1SK6 and measure the IF bandwidth -6dB points (typically $\pm$ 25-40kHz).

13) Set generator to 1.4 MHz with o/p at threshold level. Note RF millivoltmeter reading and check that all other filters are within 3dB of each other. The LSB/USB position requires the generator frequency to be offset $\pm$1kHz.

14) Set generator to 1399kHz and select 8kHz bandwidth. Adjust line level potentiometer 11RV2 for 0dBm.

15) Set signal generator to 1.4MHz 60% modulation (AM 1kHz). The AF output should be within 3dB of that obtained in SSB. Measure SINAD (16-21dB).

16) Select CW mode and BFO. Switch signal generator modulation off. Adjust BFO pitch for peak AF output (approx. 700Hz-1kHz). This should be approx. 6dB higher than the level obtained in SSB mode. Measure SINAD (25-30 dB).

N.B. Slight adjustment to BFO coil L1 / increasing the value of R34, adjacent to L1, to approx. 470 ohms (on Synthesiser board) may improve SINAD.

17) Select SSB mode, USB selectivity. Verify 2.0V present at link 2-3. Set signal generator to 1399kHz, threshold level and set a reference on the distortion factor meter.

Select AGC FAST. Increase generator o/p by 60dB>threshold level and check that audio o/p does not rise by more than 4dB. Return generator o/p to threshold level and note that the AF o/p is restored almost immediately.

Select SLOW AGC. Repeat as per FAST AGC, but observe AF o/p takes approx. 6 seconds to restore.

18) Select AUDIO AGC. Select AUDIO AGC TIME FAST. Increase generator o/p to 60dB>threshold level. Adjust 10RV5 for +2dB rise above reference level. Reduce generator o/p by 60dB and note pedestal action i.e. AF o/p is restored after approx. 2 seconds.

19) Set generator o/p to threshold level and check AF o/p remains within 1.5 dB for all AGC/manual gain settings.

20) RF AGC (perform as part of alignment of RF/1st IF except for a board check). Select AGC FAST. Connect oscilloscope to 10TP11 and increase generator o/p to 54dB>threshold level. Adjust 10RV6 to achieve 300mVpp. Adjust 10RV7 for 3V DC at 10TP12.

21) Check 600 Ohm Line o/p centre-tap (equal voltages across each half of the transformer).

22) Disconnect power from Receiver, and distortion factor meter from Ancillaries Test Box D6447. Check 600 ohm line o/p is isolated from Receiver chassis, using digital voltmeter on highest resistance range.

5.1.4 ALIGNMENT OF 1st IF BOARD

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Distortion Factor Meter with 600ohm termination.

4) Audio Power Meter (4-8ohm).

5) Ancillaries Test Box D6447.

6) Signal Generator 10kHz - 110MHz/50ohm.

7) 10 Watt RF Power Amplifier (10kHz - 30MHz).

Procedure :-

1) Connect the distortion factor meter and the audio power meter via the ancillaries test box D6447 to the ancillaries connectors 1SK4. Connect digital volt meter to 7TP4 and adjust 7RV2 for 7.5V.

2) Check 300mVpp at 7TP5. Slight adjustment to 8RV4 may be necessery.

3) Tune receiver to 1MHz. Select SSB/USB, AGC off. Adjust IF gain control for 2V at link 2-3, on Main IF audio board 10.

4) Set generator to 46.203MHz and introduce a signal at 7PL6 at a level to produce an indication on the distortion factor meter (1kHz tone).

5) Adjust 7L1 and 7L2 for max. AF o/p, reducing generator o/p to prevent overloading.

6) Connect oscilloscope to 10TP4 and adjust generator o/p to produce 500mVpp (approx. 3dBuV).

7) Check SINAD is approx. 15dB.

RF AGC adjustment

8) Select AM mode, 3kHz bandwidth. Set generator to 46.204MHz. Disconnect 22PL3 and check dc voltage at 7TP1 is approx. 0V.

9) Increase generator o/p to 54dB above the level required to produce 500mVpp at 10TP4 (6 above). This new level is the RF AGC threshold.

10) Connect oscilloscope to 10TP11 and adjust 10RV6 to obtain 300mVpp.

11) Adjust 10RV7 for 3Vdc at 10TP12. Reconnect 22PL3 and observe signal at 10TP11 does not fall by more than 1dB.

12) Connect oscilloscope to 10TP12 and check for signs of instability as generator o/p is increased by a further 54dB, in 1dB steps (i.e. approx. 112 dBuV).

Observe signal at 10TP11 has not risen >600mVpp.

13) Reset generator to RF AGC threshold level and set for 1kHz mod. depth 50%. Select AGC slow and adjust line level for 0dBm.

14) Check SINAD >38dB. Increase generator o/p by 54dB, in 1dB steps, checking that SINAD >38dB at all levels.

Over-voltage protection.

15) Fit link between board 7 pins 3-4 if a preselector is NOT fitted. Disconnect link between board 7 pins 1-2 and connect oscilloscope to pin 1.

16) Connect generator via 10Watt power amplifier (i.e. Electronic Navigation Industries 325LA) to Aerial input 1SK1. Adjust signal generator to 1MHz, modulation off and increase signal level to receiver until 'diode clipping' is observed. This occurs at approx. 6Vpp.

Repeat the above at 80kHz and 30MHz where clipping occurs at approx. 6.5Vpp and 12.5Vpp respectively.

17) Reduce input signal to a low level, disconnect supply and test equipment from receiver and solder link between pins 1-2.

18) Reconnect supply and test equipment. Slowly increase input until protection relay operates and signal at link 1-2 increases by approx. 6dB (i.e. relay 7RLA opens).

19) Reduce input until relay closes and signal at link 1-2 drops approx. 6dB. Circuit hysteresis is approx. 14dB at 80kHz. and 8dB at 30MHz.

5.1.5 ALIGNMENT OF RF AMPLIFIER BOARD

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Distortion Factor Meter with 600ohm termination.

4) Audio Power Meter (4-8ohm).

5) Ancillaries Test Box D6447.

6) Spectrum Analyser 10kHz-110MHz.

7) Two Signal Combining Pad 50ohm.

8) Signal Generator 10kHz - 110MHz/50ohm.

9) Signal Generator 10kHz - 110MHz/50ohm.

Procedure :-

1) Connect the distortion factor meter and the audio power meter via the ancillaries test box D6447 to ancillaries connectors 1SK4 and 1SK10. Adjust receiver to 1MHz, wideband, SSB mode, USB selectivity, AGC on, RF sensitivity max.

RF amplifier adjustment

2) Connect digital voltmeter to 41TP4 and adjust 41RV3 for 5Vdc. Set 41RV1 and 41RV2 central.

3) Observe first oscillator injection at 41TP3 approx. 450mVpp at 29MHz.

N.B. It is essential that a VHF oscilloscope with low capacity high impedance probes is used for this measurement. Earth leads should be kept as short as possible.

4) Introduce a signal 1.001MHz 0dBuV emf at aerial input 1SK1 and adjust line level for approx. 0dBm (1kHz tone).

5) Adjust 41RV1, 41RV2 by equal amounts to produce a SINAD of 14-15dB.

6) Two techniques for balancing the RF amplifier may be employed :-

Method 1:

Connect an oscilloscope with two low capacity probes to 41TP2 and 41TP3 and increase signal to 100dBuV emf. Display both traces and equalise the amplitude with a slight adjustment to 41RV1 and 41RV2.

N.B. As these signals are in 'anti-phase' the 'ADD' or 'SUM' facility may be utilised in order to produce a net zero result.

Method 2:

Introduce a signal at aerial input 1SK1 of 23.102MHz 80dBuv emf with the receiver tuned to 1MHz AGC off. The resulting second order intermodulation product in the RF amplifier produces the 1st IF frequency of 46.204MHz. This may be minimised with a slight adjustment of 41RV1 and 41RV2.

Ensure that a SINAD of 14-15dB for a 0dBuV emf input signal may be attained after either of these adjustments has been carried out.

Performance check
---

7) Check sensitivity as Table 5.2 which shows how sensitivity is reduced below 160kHz.

Table 5.2
Typical Sensitivity Performance

uV<---i/p--->dBuV emf	Tune Frequency	SINAD Ratio
1	0	>160kHz	>12dB
2	6	>50kHz	15dB
5	14	10kHz	15dB

8) Check SINAD with an input signal of 60dB/uV emf is >38dB on both main audio and 600ohm audio outputs.

9) Check AGC range from the threshold point. Typically a change in input of 90dB above the AGC threshold will produce less than a 3dB change in output.

10) In-band intermodulation measurement. Tune receiver to 2MHz, 8kHz bandwidth, AGC fast. Inject two signals via a combining pad at aerial input 1SK1 as Table 5.3.

Table 5.3
Intermodulation Frequencies

mV<---i/p level at receiver	emf--->dBuV	Input Frequency
200	86	2.0005MHz
200	86	1.9995MHz

11) Measure in-band intermodulation products in AGC fast and AGC slow using a spectrum analyser connected to IF o/p 1SK6 (typically >-40dB).

N.B. Where the in-band intermodulation products are high some improvement may be gained by the following slight adjustments:-

i) RF AGC threshold 10RV6 may be lowered (rotate clockwise).

ii) IF gain distrubition pot 10RV1 may be changed from it's central position.

iii) IF AGC threshold may be lowered by up to 1dB. See Section 5.1.2 and 5.1.3.

5.1.6 REAR PANEL ASSEMBLY TEST PROCEDURE

Equipment required:-

1) Digital Voltmeter.

2) 1000Vdc 'Megger' Insulation Tester.

3) AC Current Meter.

4) 10 Amp dc Constant Current Power Supply.

5) 4 off Variable Load Resistance for dc supply.

The following electrical safety checks should be carried out on a complete receiver when any Mains Supply related part has been replaced and the results compared with the orignal test results.

N.B. Replacement parts related to the Mains Supply must be exactly as those specified in the Parts List.

Electrical Safety Checks

1) ELECTRICAL STRENGTH. The insulation between the mains connector live and neutral (joined together) and the mains connector earth is measured with a dc voltage of 1000v from a 'Megger' insulation tester applied for ten seconds. The resistance must be greater than 100Mohm.

2) EARTH CONTINUITY. The earth continuity from the mains connector earth pin to the front and rear panel metalwork is tested with a current of at least 10 amps. The resistance must be less than 0.1ohm.

3) EARTH LEAKAGE. The earth leakage current must be measured, with all other earths disconnected, whilst powered from the normal mains supply. The leakage current should be less than 500uA under all conditions.

The dc supply capability may be checked by connecting loads to the four supply outputs and comparing the results as follows:-

Table 5.4
DC Supply : 'On Load' Currents

Output	Idc	+Vout	Tolerance
14PL1	400mA	15.5V	± 5%
14PL2	650mA	15.5V	
14PL4	500mA	10.5V	
14PL5	450mA	10.5V	

A typical receiver set to 28888.880kHz, wideband selected, min. AF gain, half max. display intensity and switched on for at least half an hour produces the following voltage analysis:-

Table 5.5
DC Supply : Regulator Voltage Analysis

V/Reg.	+O/P	+I/P	ref. pin
14IC1	15.3V	21.05V	14.05V
14IC2	15.25V	21.05V	14V
14IC3	10.55V	16.23V	9.31V
14IC4	10.52V	16.23V	9.28V

Table 5.6
AC Supply Inputs to Rectifier Bridges

Connector	AC voltage (on load)
14PL3	18.44V)
	) ± 5%
14PL6	14.4V)

The above assume a mains supply of 240V/50Hz and an ambient temperature of >10°C.

5.1.7 ADJUSTMENT OF INTERNAL STANDARD OSCILLATOR

Equipment Required
---

1) 'Off Air' Frequency Standard.

2) Ancillaries Test Box D6447.

3) VHF Oscilloscope with low capacity probes.

Procedure

In order to allow the internal standard oscillator accuracy to be adjusted a reference source of better than ± 0.1ppm is required. The receiver must have been 'on' for at least half an hour and have temperature stabilised in it's operational environment. A Lissajous figure technique is used to compare the receiver's internal frequency standard with the output of an 'Off Air' frequency standard. This method obviates the need for accurate frequency measuring apparatus of known standard.

1) Operate the 'Off Air' frequency standard to the manufacturer's instruction and introduce the 1MHz output to the receiver's aerial input 1SK1.

2) Connect the ancillaries test box D6447 to the receiver.

3) Tune the receiver to 29.001,000MHz (the twenty ninth harmonic + 1kHz), AGC fast, bandwidth 8kHz, SSB mode.

4) Connect the 1kHz output from the 'Off Air' frequency standard to the 'X' input on the oscilloscope and connect the 'Y' input, via the ancillaries test box D6447, to the 600 Ohm line output.

5) Adjust the oscilloscope to display a Lissajous figure (a 'square' circle) indicating a 1:1 frequency relationship.

6) Time a complete revolution of the 'square' circle which should be of the order of thirty seconds.

7) To trim the internal standard oscillator remove the 'bung' in the synthesiser cover and adjust 8RV2 with an insulated trimming tool.

8) Replace 'bung' in synthesiser cover and check receiver at other harmonics of the 1MHz input.

9) Disconnect 'Off Air' standard, ancillaries test box D6447 and oscilloscope.

5.1.8 ADJUSTMENT OF METER AND COR

1) Signal Generator 10kHz - 110MHz/50ohm.

2) Ancillaries Test Box D6447.

3) Audio Power Meter 600ohm.

RF meter adjustment

1) Connect the audio power meter to the receiver via the ancillaries test box D6447.

2) Tune the receiver to 1MHz, SSB/USB, AGC fast, meter RF, mute off, IF gain max.

3) Introduce a 1001kHz signal 50dBuV emf at 1SK1. Adjust 10RV3 on main IF board until tenth meter LED is just illuminated and check linearity in accordance with Table 5.7.

Table 5.7
RF Signal Strength LED Meter

LEDs illuminated	RF input dBuV emf
10	approx. 50
9	approx. 42
8	approx. 33
7	approx. 27
6	approx. 22
5	approx. 18
4	approx. 14
3	approx. 10
2	approx. 7
1	approx. 4

4) Switch input signal off, receiver bandwidth 16kHz and check that all LEDs are extinguished.

5) Reselect USB bandwidth and increase signal input until five meter LEDs are illuminated. Select audio AGC and observe that between four and six LEDs are on.

CZ meter

6) CZ meter is only operational when an FSK or NBFM board is fitted and is described along with these items.

COR meter

7) Tune the receiver to 1MHz, SSB/USB, AGC fast, mute on, IF gain max. select COR meter.

8) It is essential that the RF meter has been aligned prior to this procedure. Introduce a 1001kHz signal at 1SK1 sufficient to illuminate the signal LED - of the order -3dBuV emf.

9) Rotate the IF gain/mute level control anti-clockwise until ten meter LEDs are just illuminated. The signal LED is extinguished.

10) Increase the input signal until the signal LED illuminates at approx. 43dBuV-54dBuV

11) Record an output from the line amplifier with the signal LED on. Reduce the input signal until the signal LED is extinguished and observe a fall in output of approx. 20dB as the mute circuit operates.

12) Disconnect the signal generator and the ancillaries test box D6447 from the receiver.

AF line level meter calibration

13) Tune the receiver to 1MHz, SSB/USB, AGC fast, mute off, IF gain max.

14) Introduce a 1.001MHz signal 50dBuV emf at 1SK1.

15) Adjust 11RV2 for 10mW on audio power meter and 10RV8 to illuminate 7 LEDs (10mW mark) on the line level meter.

16) Adjust 10RV2 to 'working' line level (approx. 1mW) and disconnect the signal generator and the ancillaries test box D6447 from the receiver.

5.1.9 ALIGNMENT OF NBFM BOARD

(/N Receivers only)

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Distortion Factor Meter with 600ohm termination.

4) Audio Power Meter (4-8ohm).

5) Ancillaries Test Box D6447.

6) Signal Generator 10kHz - 110MHz/50ohm.

Procedure :-

1) Connect the distortion factor meter via the ancillaries test box D6447 to ancillaries connector 1SK4. Adjust receiver to 1MHz, wideband, FM mode, 16kHz selectivity, AGC FAST, CZ Meter.

2) Introduce a signal 1MHz 60dBuV emf, modulation off, at aerial input 1SK1.

NBFM adjustment

3) Set 40RV2 central and, monitoring 40IC1-8 with oscilloscope, tune 40L2 for maximum o/p (core approx. flush with top of can).

4) Connect digital voltmeter to 40TP4 and adjust 40L2 for 3.5Vdc. Adjust 40RV2 for centre deflection of CZ meter (meter LED to be just left of the 'CZ' mark).

5) Check operation of the CZ meter by increasing and decreasing the input frequency by 1-1.5kHz and observing meter moving to the extremes of it's range (meter moves left with increasing frequency).

6) Restore input frequency to 1MHz 60dBuV emf, frequency modulation 400Hz with peak deviation 3kHz.

7) Monitoring 40TP1 with oscilloscope tune 40L1 for maximum o/p.

8) Measure SINAD >30dB i.e. 3% THD.

N.B. Slight adjustment of 40C13 may improve noise performance.

9) Measure audio response as Table 5.8.

Table 5.8
NBFM Audio Response

o/p freq.	o/p level (0dBm 600ohm line)
300Hz	+1
400Hz	0
1kHz	-5.5
3kHz	-17
6kHz	-36

Squelch adjustment

10) Adjust input frequency to 1MHz -3dBuV emf, frequency modulation 400Hz with peak deviation 3kHz. Adjust 40RV1 so that the Front Panel 'Signal Lamp' is just illuminated.

11) Remove the input signal and check that the 'Signal Lamp' is extinguished.

5.1.10 ALIGNMENT OF FSK BOARD

(/K Receivers only)

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Audio Oscillator 10Hz - 20kHz.

4) Signal Generator 10kHz - 110MHz/50ohm.

5) 15.5Vdc Regulated Power Supply.

Procedure :-

FSK Module Test

1) Remove FSK PCB from receiver as described in Section 5.2.14 FSK BOARD.

2) Connect 15.5Vdc supply to FSK board 42PL1-2 and to FSK ON/$\overline{\text{OFF}}$ input 42PL1-4 and check the outputs of both voltage regulators.

42IC5 = +8V)
) ± 5%
42IC8 = +5V)

3) Short circuit audio input 42PL1-6 to ground and and monitor 42TP2 with digital voltmeter. Set 42RV3 central and adjust 42RV2 for 6.6Vdc (±0.1Vdc).

4) Monitor 42TP3 with digital voltmeter and adjust 42RV3 so that the former is the same as 42TP2 i.e. 6.6Vdc (±0.1Vdc).

5) Iterate steps 3 and 4 until interaction ceases.

6) Disconnect FSK ON/$\overline{\text{OFF}}$ input and check that the voltage at either 42TP2 or 42TP3 falls to 5.5Vdc (±0.25Vdc) depending upon the setting of switch 42SW1 and that the alternate 'Test Point' remains at 6.6Vdc.

7) Reconnect FSK ON/$\overline{\text{OFF}}$ input to 15.5Vdc power supply. Remove short circuit across audio input and introduce 1.7kHz (±10Hz) sinewave from audio oscillator at 42PL1-6. Monitoring output at 42IC1-5 with oscilloscope, increase audio input until limiting is observed at approx 700mVpp for an input

of 20mVpp (≠30mVpp).

8) Observe 600-800mVpp at 42IC4-5 for an input of 100mVpp.

9) Peak output 42IC4-13 with 42RV1 approx. 400-500mVpp.

10) Monitoring 42TP4 with an oscilloscope, check that the setting of 42RV1 (step 9) coincides with the 0/5V switching point - slightly re-adjust 42RV1 if necessary (checking setting of 42RV3 first i.e. steps 3-5).

11) Monitor FSK output at 42PL2-1, meter output at 42TP1 and check performance as Table 5.9.

Table 5.9
FSK/Meter Output Levels

Input Freq.	Output Level	Meter o/p (42TP1)
>1.7 - 3.0kHz	-10V ±1V	0V (42RV4 central)
<1.7 - 1.0kHz	+10V ±1V	5V (42RV4 central)

The switching point should be 'clean' and free from instability.

FSK Module Test in Receiver

12) Install FSK PCB in receiver as described in Section 5.2.14 FSK BOARD.

13) Select FSK (FM) Mode, AGC Fast, Max Sens. and adjust receiver to 1MHz with BFO at +1.7kHz.

14) Monitor FSK output at Remote Connector 1PL1-1 with oscilloscope.

15) Select CW Mode and check that the output is static i.e. no transitions. Check that switch 42SW1 inverts the output level - leave at -10Vdc (42SW1 away from PCB edge).

16) Select FSK(FM) Mode. Introduce a signal of 1MHz 10dBuV emf, 80Hz deviation (160Hz shift), externally modulated with 25Hz square wave (approx. 50Baud) at 1SK1.

17) Observe 1:1 MARK/SPACE ratio adjusting 42RV1/3 as required.

18) Select Meter CZ and adjust 42RV4 so that the

fifth LED is illuminated for a 1:1 MARK/SPACE ratio. Adjust tuning (Rx) and observe change in meter reading with corresponding change in MARK/SPACE ratio.

19) Re-tune receiver to 1MHz and reduce input signal until output waveform starts to 'break up' at approx. -10dBuv.

20) Observe that an increase in signal level to approx. 60dBuv produces no significant change in MARK/SPACE ratio.

21) Decrease signal level to 10dBuV and increase modulation frequency to 150Hz (300 Baud) and observe no significant change in output MARK/SPACE ratio.

22) Increase deviation to 500Hz (1kHz shift) and decrease modulation to 100Hz (200 Baud) and observe no significant change in output MARK/SPACE ratio.

23) Disconnect signal generator and oscilloscope from receiver and perform 'off air' tests using teleprinter.

5.1.11 ALIGNMENT OF EXTERNAL STANDARD BOARD

(/S Receivers only)

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Signal Generator 10kHz - 110MHz/50ohm.

Procedure :-

1) Check power supply 15.5V present at connector 1SK1-4 (flying lead).

2) Observe 5.6MHz 15Vpp with oscilloscope at 1SK1-1.

3) Make link between pins 5 and 6 i.e. 1MHz operation and introduce a 1MHz signal, 500mVpp at 17PL1-1.

4) Monitor output at 17TP3 with oscilloscope and observe 1Vpp, Observe AGC action of 17IC6 (SL1610).

5) Adjust 17RV1 so that External Standard LED on Front Panel is just illuminated for 500mVpp input at 17PL1-1.

6) Remove 1MHz input and observe the External Standard LED extinguished.

7) Select BITE mode on receiver and select BITE test 04. 'PASS' is displayed with 1MHz signal present and 'SPARE' is displayed with 1MHz signal absent.

8) Check that 'offtuning' the 1MHz input at 17PL1-1 by ±20Hz causes BITE test 04 to display 'FAIL'.

5.1.12 FRONT PANEL ASSEMBLY MICROCOMPUTER

Refer to circuit diagrams BP1953 and BP1992 bound at rear.

Equipment required

1) VHF Oscilloscope. Greater than 120MHz bandwidth, dual channel with 50 Ohm and high impedance inputs on both channels. High impedance approximately 10 Mohm in parallel with 7pF (using a 10x probe).

2) EP8000 EPROM Emulator. With BSC-8 Buffered Simulator Cable (G.P. Industrial Electronics) (EM/SC).

3) Front Panel Test Box D6247.

4) Regulated Power Supply +15.5V/5A.

Initial Checks

The following checks are of the basic Microcomputer Board 'internal' control signals.

Step 1. Remove the front panel assembly from the receiver (see section 5.2.2).

Step 2. Access the Microcomputer Board (see section 5.2.4).

Step 3. Connect Front Panel Test Box D6247 to 12PL1 and a +15.5V regulated power supply.

Step 4. Check that the output of voltage regulator 13IC14 (MC7805CT) is in the range 4.75 to 5.25V dc.

Step 5. Check that pin 4 of 13IC15 (MCT2) goes high when the Microcomputer power supply, via pin 4 of 12PL1, exceeds a maximum of 9.8V and goes low when the supply falls below a minimum of 8.5V. Note that the supply to the Microcomputer Board is via diode 12D3.

Step 6. Check that each time the supply rises above the upper level found in step 5, an approximately 0.1 to 0.25 second low going RESET pulse is generated at the collector of 13TR1 (BC547B). Note that this level can be checked at pin 1 Of 13PL2. This is a useful initial check if a Microcomputer/control fault is suspected, since pin 1 of 13PL2 can easily be accessed by just removing the top dust cover of the complete receiver and then

generating the RESET pulse by connecting the mains power supply.

Step 6. Check the enable pulses at 13TP1/2/3.

EPROM Verification

If a control fault is suspected, the programs stored in the two Microcomputer Board EPROMs can be checked as follows. Note that the Microcomputer Board has two EPROMs, 12972P and 12973P, each with a different stored program, and that to check these, a known good EPROM of each program type will be required. Generally three such EPROMs of each type should be retained to enable verification of the known good EPROMs themselves by comparison against each other (a faulty one would be recognised as being different from the other two).

Step 1. Remove the front panel assembly from the receiver (see section 5.2.2).

Step 2. Access the Microcomputer Board (see section 5.2.4).

Step 3. OBSERVING THE USUAL ANTI-STATIC PRECAUTIONS carefully remove the two EPROMs, 13IC8 and 13IC9, from their sockets and store them on conductive foam pads.

Step 4. Obtain a known good EPROM of each program type.

Step 5. Select '2764 A' on the EP8000 by pressing <FN>, <DEV> and using its up and down cursor keys as necessary.

Step 6. Press <RST> on the EP8000 and ensure the green power indicator above the zero insertion force (ZIF) socket on the EP8000 is off.

Step 7. Carefully insert one of the known good EPROMS into the 28 pin ZIF socket with pin 1 towards the top left-hand side. Press <FN>, <STOR> to transfer its contents into the EP8000.

Step 8. Press <RST> again and remove the known good EPROM replacing it with the equivalent suspect EPROM from the receiver.

Step 9. Press <FN>, <VFY> to check the contents of the suspect EPROM with that of the known good EPROM now stored in the EP8000. A 'PASS' display indicates

the suspect EPROM is correct, a 'FAIL' display indicates it is faulty.

Step 10. Repeat with the other receiver EPROM and known good EPROM remembering to press <RST> each time before loading or unloading the ZIF socket to ensure power to the socket is first removed.

Address Strobe Checks

The Microcomputer generates strobe pulses for various control ICs on the Microcomputer Board itself and on the Interface Board. The functions of these ICs are detailed in 'SECTION 4 : CIRCUIT DESCRIPTION' and in the following section. The Interface Board circuit diagram BP1992, bound at rear, also indicates the general functions of the Interface Board control ICs (pins 10 to 17 inclusive of 13PL3/12SK2). If a fault occurs in a particular control operation, the address strobes to the associated ICs should be checked. For example, for faulty keyboard operation, the address strobes to 12IC15 and 12IC16 should be checked via pins 10 (READ KEYBOARD '2007') and 11 (WRITE KEYBOARD '2006'), respectively, of 13PL3/12SK2, through to pin 15 of 12IC14 or pin 11 of 12IC16. A method of generating regular address strobes, which can be easily monitored on an oscilloscope, is given as follows. Note that each control IC has a its own numerical address ('2007' and '2006' in the previous example) which is given on circuit diagram BP1992.

Step 1. Remove the front panel assembly from the receiver (see section 5.2.2).

Step 2. Access the Microcomputer Board (see section 5.2.4).

Step 3. OBSERVING THE USUAL ANTI-STATIC PRECAUTIONS carefully remove the two EPROMs, 13IC8 and 13IC9, from their sockets and store them on conductive foam pads.

Step 4. Ensuring that it is not switched on, connect the EP8000 via the BSC-8 buffered simulator cable to the EPROM socket for 13IC9. Note that the BSC-8 requires the 28 pin lead option and requires internal switch settings to be made for 2764A type EPROMS. Ensure, in particular, that the connector is fitted into the EPROM socket correctly (pin 1 of the cable plug to the marked end of the EPROM socket). It is advisable to use an intermediate socket between the emulator plug and the board socket in order to avoid damage to the latter by large pins.

Step 5. Switch the EP8000 on and select '2764A' by pressing <FN>, <DEV> and using its up and down cursor keys as necessary. Press <RST> and enter the short program, given in Table 5.7, into the EP8000. The control IC function, the associated address and test points are given in Table 5.8.

Step 6. Press <DMA> on the EP8000 and apply +15.5V to 12PL1 pin 10, +10.5V to 12PL1 pins 4 and 6, ground returns to pins 9, 5 and 7 respectively (Interface Board). The Microcomputer should RESET and run just the short simple test program entered into the EP8000. This program just does a repetitive load from the specified address simply to obtain a repetitive address strobe pulse, the actual loading being inconsequential.

Step 7. Monitor the appropriate test point, in Table 5.8, where the waveforms shown in Figure 5.4 or 5.5 should be found.

Figure 5.4
Address Strobe Test (1)

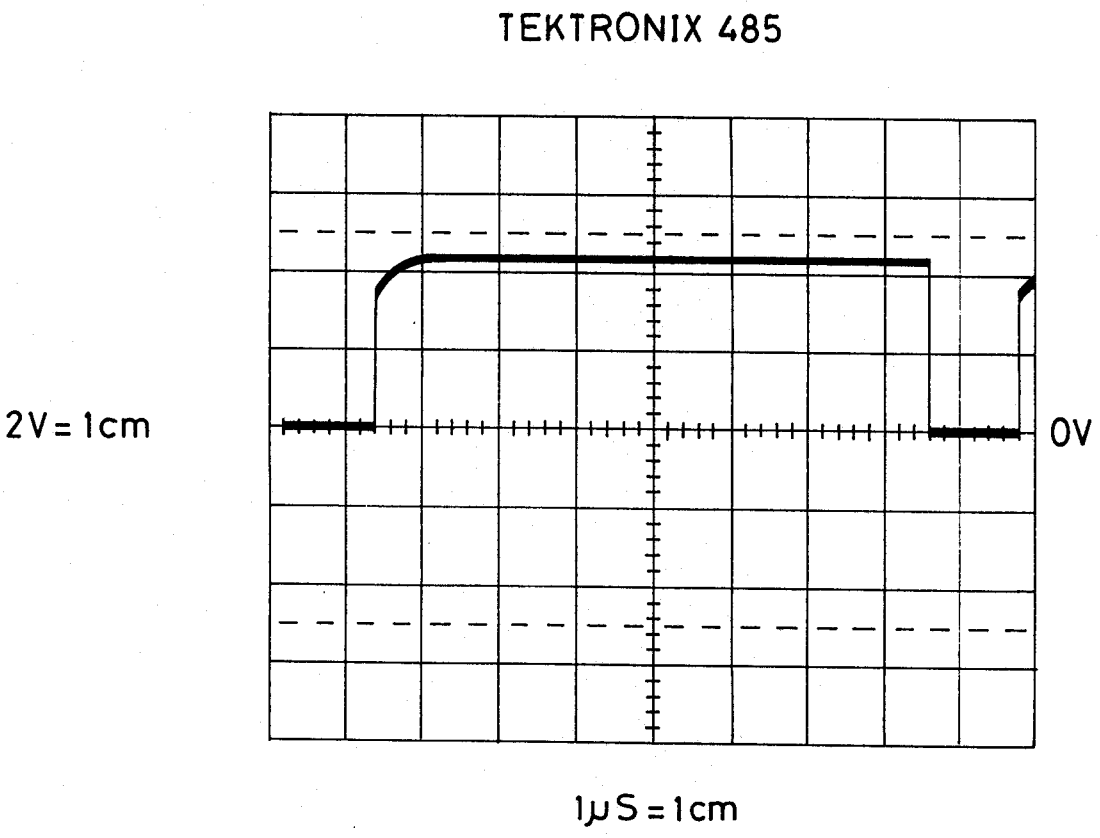
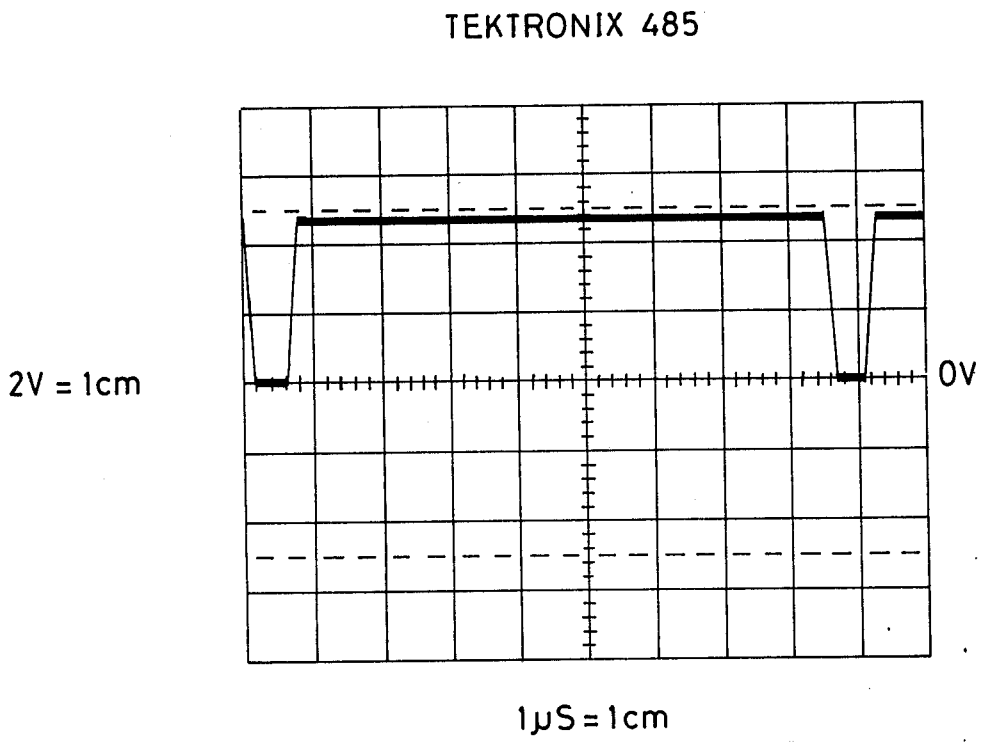


Figure 5.5
Address Strobe Test (2)



Step 8. If a check of another address strobe is required, first remove all power to the Interface Board, press <DMA> on the EP8000, replace the original address in the EP8000 program (xxyy) with the new address, press <DMA> again and re-apply power to the Interface Board.

Table 5.10
Address Strobe Test Program

Address	Code	Mnemonic
3000	B6	LDAA
3001	xx	see Table 5.8
3002	yy	see Table 5.8
3003	7E	JMP
3004	E0	back to prog-
3005	00	ram start
:		
:		
:		
4FFE	E0	RESET
4FFF	00	Vector

Table 5.11
Function Address xxyy

Function	xxyy	Monitor Points/Waveform
2Kbyte RAM	0000	pin 15 of 13IC13 / Fig 5.4 pin 18 of 13IC5 / Fig 5.5
D/A Write Meter Dot/Bar	2000	pin 14 of 13IC13 / Fig 5.4 pins 4/5 of 13IC3 / Fig 5.4
Tuning knob, Pre-selector motor control	4000	pin 13 of 13IC13 / Fig 5.4 pin 15 of 13IC1 / Fig 5.4
2nd EPROM	C000	pin 9 of 13IC13 / Fig 5.4 pin 18 of 13IC8 / Fig 5.4
A/D Read	2001	pin 14 of 13IC3 / Fig 5.5 pin 16 of 13PL3/12SK2 pin 2 of 12IC10 / Fig 5.5
RF/IF Write	2002	pin 13 of 13IC3 /Fig 5.5 pin 15 of 13PL3/12SK2 pin 11 of 12IC6 / Fig 5.5
Status/Remote Read	2003	pin 12 of 13IC3 / Fig 5.5 pin 14 of 13PL3/12SK2 pins 1/15 of 12IC4 /Fig 5.5
Synthesiser Write	2004	pin 11 of 13IC3 / Fig 5.5 pin 13 of 13PL3/12SK2 pin 11 of 12IC7 / Fig 5.5
Display and Remote Write	2005	pin 10 of 13IC3 / Fig 5.5 pin 12 of 13PL3/12SK2 pin 11 of 12IC7 / Fig 5.5
Keyboard Write /Setup	2006	pin 9 of 13IC3 / Fig 5.5 pin 11 of 13PL3/12SK2 pin 11 of 12IC16 / Fig 5.5
Keyboard Read	2007	pin 7 of 13IC3 / Fig 5.5 pin 10 of 13PL3/12SK2 pins 1/15 of 12IC14/15 / Fig 5.5

5.1.13 FRONT PANEL ASSEMBLY CONTROL FUNCTIONS

Refer to circuit diagrams BP1953, BP1992 and BP1996 bound at rear.

Front Panel Controls

Operation of all front panel controls (except 'AF GAIN' and 'LINE LEVEL') and displays can be verified with the front panel assembly removed from the receiver. Details of the operation of each control are given in section 3.1 'Controls'. Correct operation of the corresponding receiver circuitry however, can obviously only be verified with the assembly connected to the receiver. If correct operation is not obtained in this circumstance, then the fault may lie in the Interface Board control ICs or serial to parallel converters. Table 5.9 indicates the ICs used to control the various receiver sections. If a fault is suspected in the control of a section, the appropriate ICs can be checked for digital logic level activity at their outputs (inputs are generally in common). To gain better access to the Interface Board, the front panel assembly can be moved to its 'forward' test position (see section 5.2.1 Front Panel Access). It is important before any 'logic analysis' takes place on either the Interface or Display boards that the voltage regulator 12IC8 (5V) is checked and the supply to all associated integrated circuits.

Table 5.12
Control Integrated Circuits

Section	Control via -
Synthesiser	12IC7 and connector 12RS3
Pre-selector and RF/1st IF	12IC6, 12IC3. Pre-selector motor driven gang via pulse on pin 11 of 13PL2/12SK1 and pin 4 of connector 12RS4.
Main IF /Audio	12IC6, 12IC4, 12IC3 and 12IC2
Display and Remote output	12IC7
Remote input	12IC5

Table 5.12 (continued)

Section	Control via -
Synth. unlock, Ext. Std. Lock Mute/Signal	12IC4
Keyboard	12IC14, 12IC15 (Read), 12IC16 (Write)
Main Tuning Knob	Pulses from knob via pin 2 of 12RS5 and pin 7 of 13PL2/12SK1 when knob turned clockwise ('up'). Pulses from knob via pin 1 of 12RS5 and pin 4 of 13PL2/12SK1 when knob turned anti-clockwise ('down').

Output Control IC Tests

If faults are suspected in output control ICs 12IC6, 12IC17 or 12IC16 and the address strobes to them have been checked (see previous section 5.1.9), the test program given can be modified to check that the outputs of these ICs are functioning. The full procedure is as follows.

Step 1. Remove the front panel assembly from the receiver (see section 5.2.2).

Step 2. Access the Microcomputer Board (see section 5.2.4).

Step 3. OBSERVING THE USUAL ANTI-STATIC PRECAUTIONS carefully remove the two EPROMs, 13IC8 and 13IC9, from their sockets and store them on conductive foam pads.

Step 4. Ensuring that it is not switched on, connect the EP8000 via the BSC-8 buffered simulator cable to the EPROM IC socket for 13IC9. Note that the BSC-8 requires the 28 pin lead option and requires internal switch settings to be made for 2764 type EPROMS. Ensure, in particular, that the connector is fitted into the EPROM socket correctly (pin 1 of the cable plug to the marked end of the EPROM socket). It is advisable to use an intermediate socket between the emulator plug and the board socket to avoid damaging the latter by large pins.

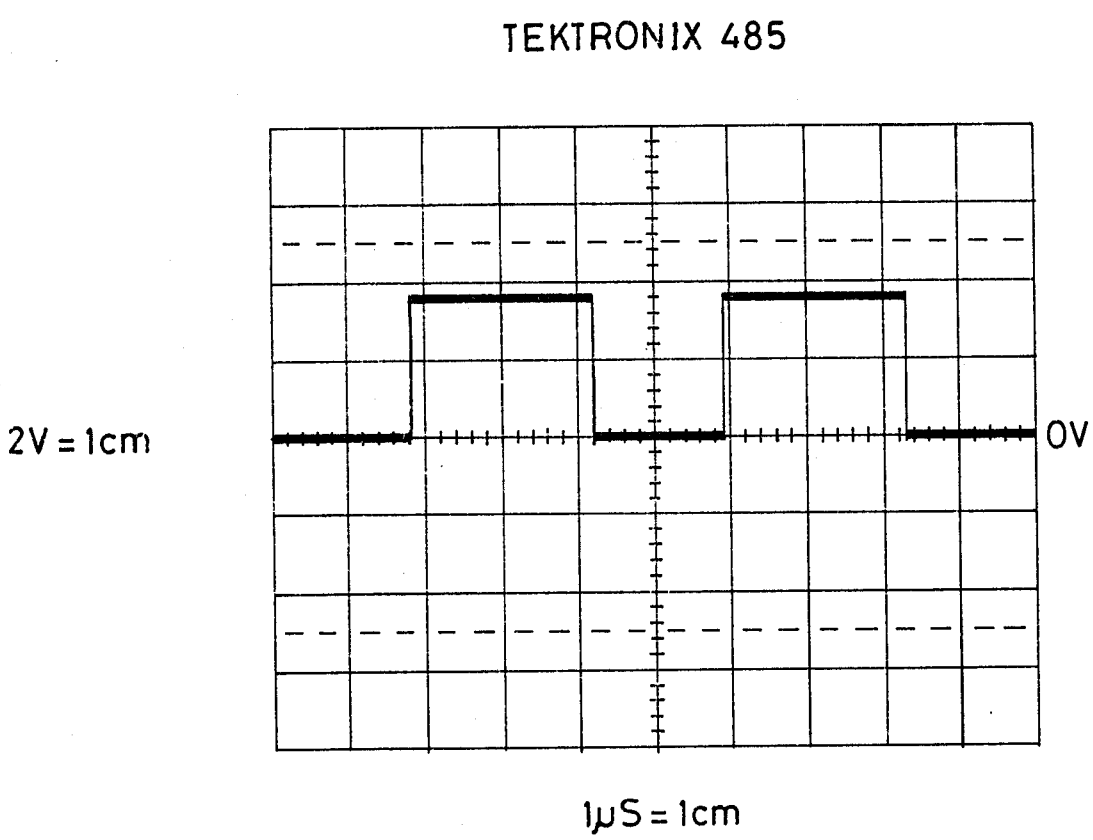
Step 5. Switch the EP8000 on and select '2764 A' by pressing <FN>, <DEV> and using its up and down

cursor keys as necessary. Press <RST> and enter the short program, given in Table 5.10, into the EP8000. The output control IC function, the associated address and test points are given in Table 5.11.

Step 6. Press <DMA> on the EP8000 and apply +15.5V to 12PL1 pin 10, +10.5V to 12PL1 pins 4 and 6, ground returns to pins 9, 5 and 7 respectively (Interface Board). The Microcomputer should RESET and run just the short simple test program entered into the EP8000. This program just does a repetitive load of alternating data into the selected IC's outputs.

Step 7. Monitor the appropriate test point, in Table 5.11, where the waveforms shown in Figure 5.6 should be found.

Figure 5.6
Output Control Test



Step 8. If a check of another output IC is required, first remove all power to the Interface Board, press <DMA> on the EP8000, replace the original address in the EP8000 program (xxyy) with the new address, press <DMA> again and re-apply power to the Interface Board.

Table 5.13
Output Control IC Test Program

Address	Code	Mnemonic
3000	86	LDA#
3001	55	01010101
3002	B7	STAA
3003	xx	see Table 5.11
3004	yy	see Table 5.11
3005	86	LDAA
3006	AA	10101010
3007	B7	STA#
3008	xx	as above
3009	yy	as above
300A	7E	JMP
300B	E0	back to prog-
300C	00	ram start
:		
:		
:		
4FFE	E0	RESET
4FFF	00	Vector

--oOo--

Table 5.14
Output IC Address xxyy

Function	xxyy	Monitor Points
Synthesiser Write	2004	pins 2, 5, 6, 9, 12, 16, 19, of 12IC7. Pins 3 and 5/10 inc of 12RS3
Display and Remote output	2005	pins 2, 5, 6, 9, 12, 17, 15, 16, 19, of 12IC10. Pins 1/2 of 12PL4.
Keyboard Write and receiver settings	2006	pins 2, 5, 6, 9, 12, 15, 16, 19, of 12IC16 Pins 1/6 inc. of 12PL5

Input Control IC Tests

If faults are suspected in input control ICs 12IC4, 12IC5 or 12IC15 and the address strobes to them have been checked (see previous section 5.1.9), the test program given can be modified to check that the inputs of these ICs are functioning. The full procedure is as follows.

Step 1. Remove the front panel assembly from the receiver (see section 5.2.2).

Step 2. Access the Microcomputer Board (see section 5.2.4).

Step 3. OBSERVING THE USUAL ANTI-STATIC PRECAUTIONS carefully remove the two EPROMs, 13IC8 and 13IC9, from their sockets and store them on conductive foam pads.

Step 4. Ensuring that it is not switched on, connect the EP8000 via the BSC-8 buffered simulator cable to the EPROM IC socket for 13IC9. Note that the BSC-8 requires the 28 pin lead option and requires internal switch settings to be made for 2764 type EPROMS. Ensure, in particular, that the connector is fitted into the EPROM socket correctly (pin 1 of the cable plug to the marked end of the EPROM socket). It is advisable to use an intermediate socket between the emulator plug and the board socket in order to avoid damaging the latter by large pins.

Step 5. Switch the EP8000 on and select '2764 A' by pressing <FN>,<DEV> and using its up and down cursor keys as necessary. Press <RST> and enter the short program, given in Table 5.12, into the EP8000. The control IC function, the associated address and test points are given in Table 5.13.

Step 6. Press <DMA> on the EP8000 and apply +15.5V to 12PL1 pin 10, +10.5V to 12PL1 pins 4 and 6, ground returns to pins 9, 5 and 7 respectively (Interface Board). The Microcomputer should RESET and run just the short simple test program entered into the EP8000. This program just does a immediate repetitive transfer of an input IC's settings to the output of 12IC17 where they can be monitored.

Step 7. Monitor the 'DO' output of 12IC17 (pin 19) with the oscillocsope, and short the 'DO' input of the selected input IC to ground. The 'DO' output of 12IC17 should fall to a logic zero (less than 0.5V). Remove the short on the selected input IC and the 'DO' output of 12IC17 should immediately rise to a

logic one (greater than 2.4V). Repeat this using the 'D1' to 'D5' inputs monitoring the 'D1' to 'D5' outputs respectively. Shorting points for specific control functions are given in Table 5.13.

Step 8. If a check of another input IC is required, first remove all power to the Interface Board, press <DMA> on the EP8000, replace the original address in the EP8000 program (xxyy) with the new address, press <DMA> again and re-apply power to the Interface Board.

Table 5.15
Input Control IC Test Program

Address	Code	Mnemonic
3000	B6	LDAA
3001	xx	see Table 5.8
3002	yy	see Table 5.8
3003	B7	STAA
3004	20	Output IC
3005	05	12IC10
3006	7E	JMP
3007	E0	back to prog-
3008	00	ram start
:		
:		
:		
4FFE	E0	RESET
4FFF	00	Vector

--oOo--

Table 5.16
Input IC Address xxyy

Function	xxyy	Shorting Points
Serial Input	2003	pin 12 of 12IC5 or pin 3 of 12PL3 ('D0' monitored at pin 19 of 12IC17)
Scan/Sweep Hold	2003	pin 14 of 12IC5 or pin 2 of 12PL3 ('D1' monitored at pin 2 of 12IC17)

Table 5.16 (continued)

Function	xxyy	Shorting Points
Ext. DC	2003	pin 2 of 12IC4 or pin 1 of 12PL3 ('D2' monitored at pin 16 of 12IC17)
Ext. Std. Lock	2003	pin 10 of 12IC4 or pin 2 of 12PL2 ('D3' monitored at pin 5 of 12IC17)
BFO Unlocked	2003	pin 6 of 12IC4 or pin 4 of 12RS3 ('D4' monitored at pin 15 of 12IC17)
Main Loop Unlocked	2003	pin 12 of 12IC4 or pin 1 of 12RS3 ('D5' monitored at pin 6 of 12IC17)
Mute/Signal	2003	pin 14 of 12IC4 or pin 2 of 12RS1 ('D7' monitored at pin 9 of 12IC17)
Keyboard Read	2007	pins 2, 14, 12, 6, 10 of 12IC15 and pin 14 of12IC14 or pins 14/8 inc. of 12PL5 ('DO/D6' inc. monitored at pins 19, 2, 16, 5, 15, 6, 12, of 12IC17)
A/D Converter Read	2001	Varying the voltage at 12TP4 will vary the state of pins 13/20 inc. of 12IC10. A similar state 'DO/D6' may be monitored at pins 19, 2, 16, 5, 15, 6, 12 of 12IC17

5.1.14 ALIGNMENT OF RF PRE-SELECTOR

(/A Receivers only)

Equipment required:-

1) Digital Voltmeter.

2) VHF Oscilloscope with low capacity probes.

3) Distortion Factor Meter with 600ohm termination.

4) Capacity Measuring Bridge, Range 15pF - 400pF

5) Ancillaries Test Box D6447.

6) Signal Generator 10kHz - 110MHz/50ohm.

The alignment may be split into two stages :-

i) Mechanical alignment of the motor-gearbox-gang assembly and electrical setting of the associated servo circuitry. This should only be attempted if a part of the said circuitry or assembly has been replaced resulting in the original settings being lost.

ii) Alignment of ranges (except the low pass filter which requires no adjustment).

Mechanical Alignment

1) With the supply removed - disconnect the four relay boards from the pre-selector unit and connect the capacity bridge across a section of the tuning gang. Connect the bridge as near as possible to the gang stator in order to minimise stray capacity.

2) Connect the distortion factor meter and the audio power meter via the ancillaries test box D6380 to ancillaries connectors 1SK4 and 1SK10 and reconnect the supply. Adjust receiver to wideband on, SSB mode, USB selectivity, AGC on, RF sensitivity max.

3) Set potentiometer 2RV2 to central position, ensure that all coupler screws in A, B, C and D couplers (Figure 5.7) are loose and ensure wiring from board to servo potentiometer 2RV1 is as Figure 5.8 (if wiring has been disconnected previously).

N.B. On no account should the servo potentiometer 2RV1 be continuity tested with a current higher than 1mA in order to avoid 'marking' the resistance track.

Figure 5.7
Pre-selector Coupler Positions

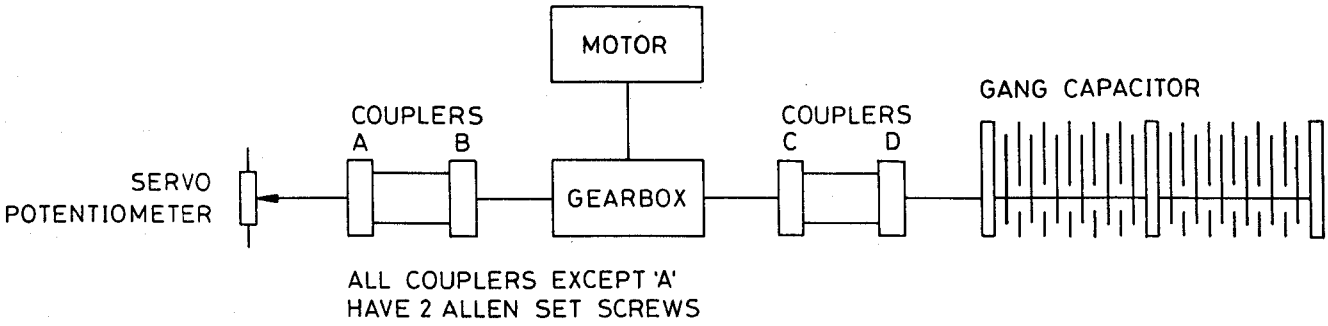
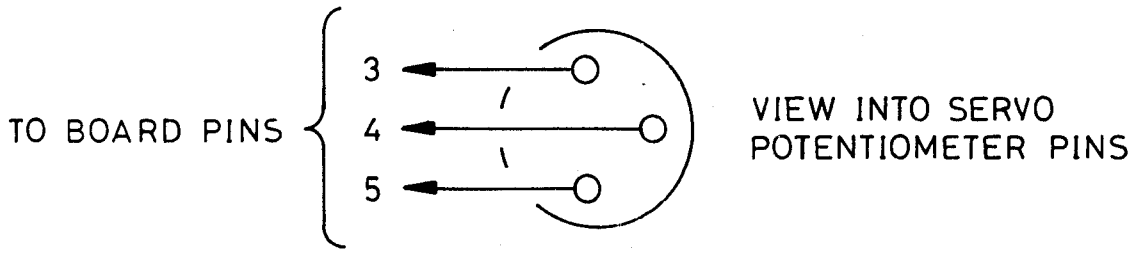


Figure 5.8
Servo Potentiometer Wiring



4) Ensure that board pin 3 is approx. 2.5V.
Ensure that board pin 5 is approx. 1.1V.
Ensure that board pin 4 varies between 1.1V and 2.5V as 2RV1 is turned.

5) Tighten screws in couplers A and B and check that each gang section is approx. 15pF minimum and 378pF maximum. Rotate manually to achieve this.

6) De-select 'Wideband' i.e. pre-selector on and tune to 585kHz. The motor will settle in a certain position. Set the gang to approx 36pF per section and lightly tighten couplers C and D.

7) Tune to 296kHz and observe gang turning to near max. capacity. If the gang is fully meshed i.e. 'end stopped' tune up from 296kHz with the control knob and adjust 2RV2 so that at 296kHz a capacity of 365pF per gang section may be achieved.

8) Iterate 6) and 7) until both capacities are attained. The mechanical adjustment at 585kHz provides the 'set point' while adjustment of 2RV2 at 296kHz provides the 'range'.

9) Verify capacity 311pF at 315kHz and 118pF at 450kHz.

10) The 5V control pulse from the microcomputer may be measured at the non-earthy end of 2R22 (47k).

315kHz	585kHz	Pulse Rep. Freq.
1.2mS	1.8mS	40mS

11) Tighten all screws in couplers A, B, C, and D, disconnect the supply and refit all circuit boards.

12) Connect supply and verify operation.

Range Alignment

13) Ranges one to eight are aligned in a conventional manner using the tracking points given in Table 5.14. Figure 5.9 shows positions of trimmers and coil cores. Trimmers should be peaked at the appropriate HF tracking points and coil cores at the LF tracking points. Insertion loss should be compared to 'Wideband' at these points and the tracking check point and not be greater than 6dB.

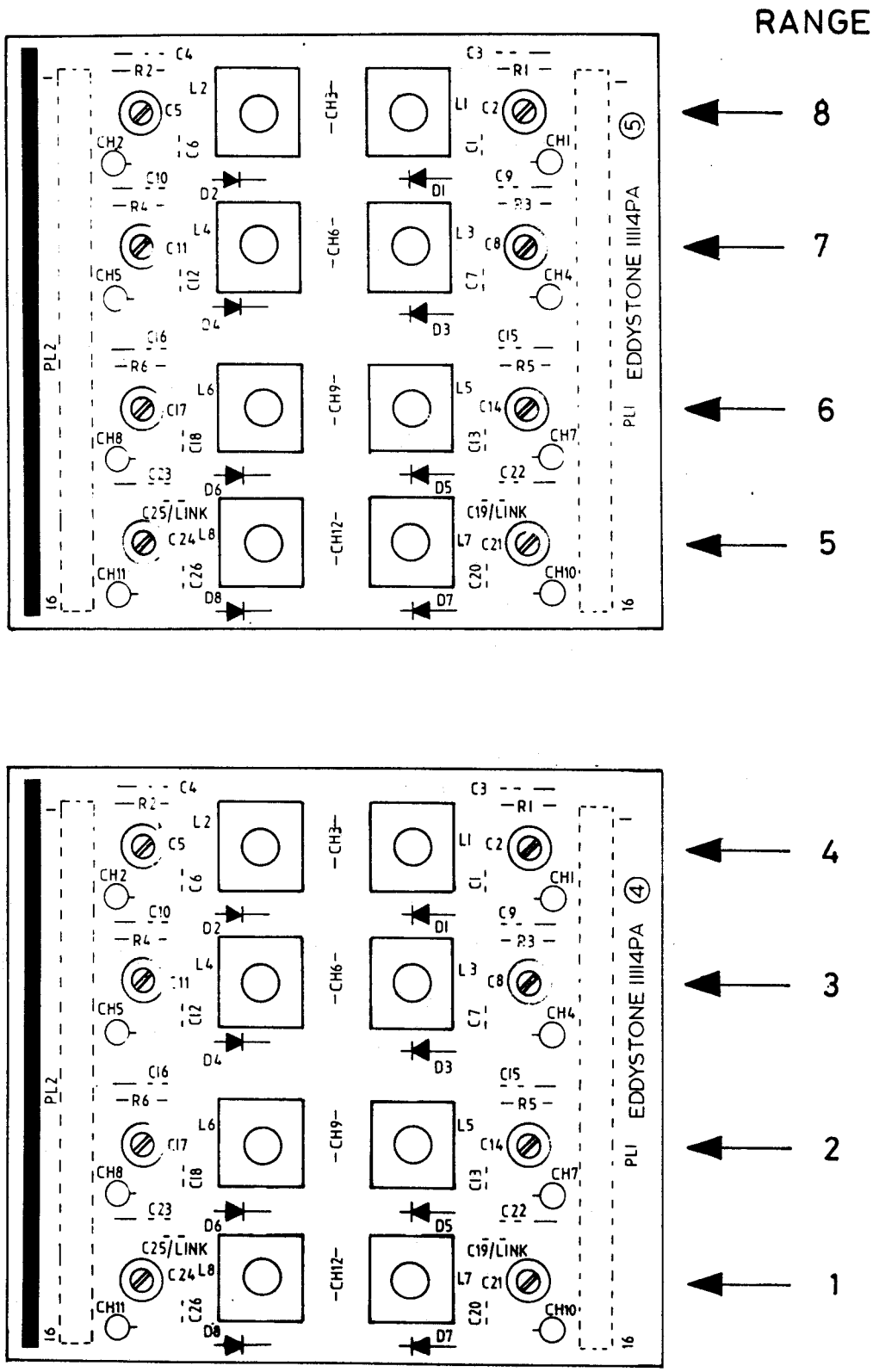
Table 5.17
Pre-selector Tracking Points

Range	HF Track	LF Track	Tracking Check Point
8	292kHz	158kHz	250kHz
7	585kHz	315KHz	510kHz
6	1170kHz	620kHz	1000kHz
5	2430kHz	1240kHz	2140kHz
4	4900kHz	2600kHz	4200kHz
3	9800kHz	5100kHz	8600kHz
2	19500kHz	10300kHz	18500kHz
1	29500kHz	20400kHz	28000kHz

Finally check 'Range 9' insertion loss (compared to 'Wideband' selected at 148kHz, 100kHz, 50kHz and 10kHz). Insertion loss should not exceed 6dB at any point.

N.B. The receiver does not have to be exactly set to the above frequencies to obtain correct alignment (within ±2kHz is satisfactory). When adjusting at the HF tracking point, or checking at the 'Tracking Check Point' rock gang side to side, (by lightly easing couplers C/D to either side) to ensure setting from either direction of 'rock' produces a 'peaked' output within 1dB.

Figure 5.9
Position of Trimmers and Coil Cores



5.2 MODULE ACCESS AND REMOVAL

5.2.1 FRONT PANEL ACCESS

1) Remove top and bottom dust covers.

2) Loosen M4 fixing screw in either sidepanel slot and remove the other two allowing the front panel to slide forward into it's 'forward test position'. Tighten fixing screw in either sidepanel slot.

3) This position is also recommended for use when inserting or removing connections to this assembly.

5.2.2 FRONT PANEL ASSEMBLY

1) See section 5.2.1.

2) Disconnect all leads to the assembly and remove both sidepanel M4 fixing screws.

3) Slide front panel forward clear of receiver and support either on it's handles or on the side panel brackets.

N.B. Take care not to damage the membrain switch top or bottom edge.

5.2.3 INTERFACE BOARD

1) See section 5.2.2.

2) Carefully disconnect membrain switch tail at 12PL5 keeping the connector faces parallel throughout.

3) Disconnect ribbon connectors 12RS5 and 12RS6 and remove five M3X16 fixing pillars and washers.

4) Withdraw interface board and microcomputer assembly from studs.

5.2.4 MICROCOMPUTER ASSEMBLY

1) See section 5.2.3.

2) Remove cover held by two M3X6 hexscrews.

3) Disconnect 13PL1 and remove two M3X20 fixing pillars and washers holding PCB and one locating heatsink.

4) Very gently prise apart 13PL2/12SK1 and 13PL3/12SK2 keeping the connector faces parallel throughout.

N.B. Sockets 12SK1 and 12SK2 must remain at right angles to the printed circuit board at all times in order to avoid strain and possible 'track fracture'.

5) Withdraw microcomputer board from studs.

Re-assembly

Re-assembly is the reverse of the above except where the microcomputer board is to be fitted to another interface board. This will require the microcomputer box to be re-aligned (see Figure 5.4/5/6) as follows:-

6) Loosen four M3 hexscrews allowing microcomputer box to'float'.

7) Install microcomputer board taking care that the connector faces 13PL2/12SK1 and 13PL3/12SK2 are parallel throughout and at right angles to the interface board.

8) Orientate microcomputer box so that the board fixing studs are centralised in the fixing holes.

9) Tighten four M3 hexscrews fixing microcomputer box.

10) Replace two M3X20 fixing pillars and washers holding PCB and one locating heatsink and connect 13PL1.

11) Reconnect 13PL1 and replace microcomputer box lid.

Figure 5.10
Microcomputer Alignment (1)

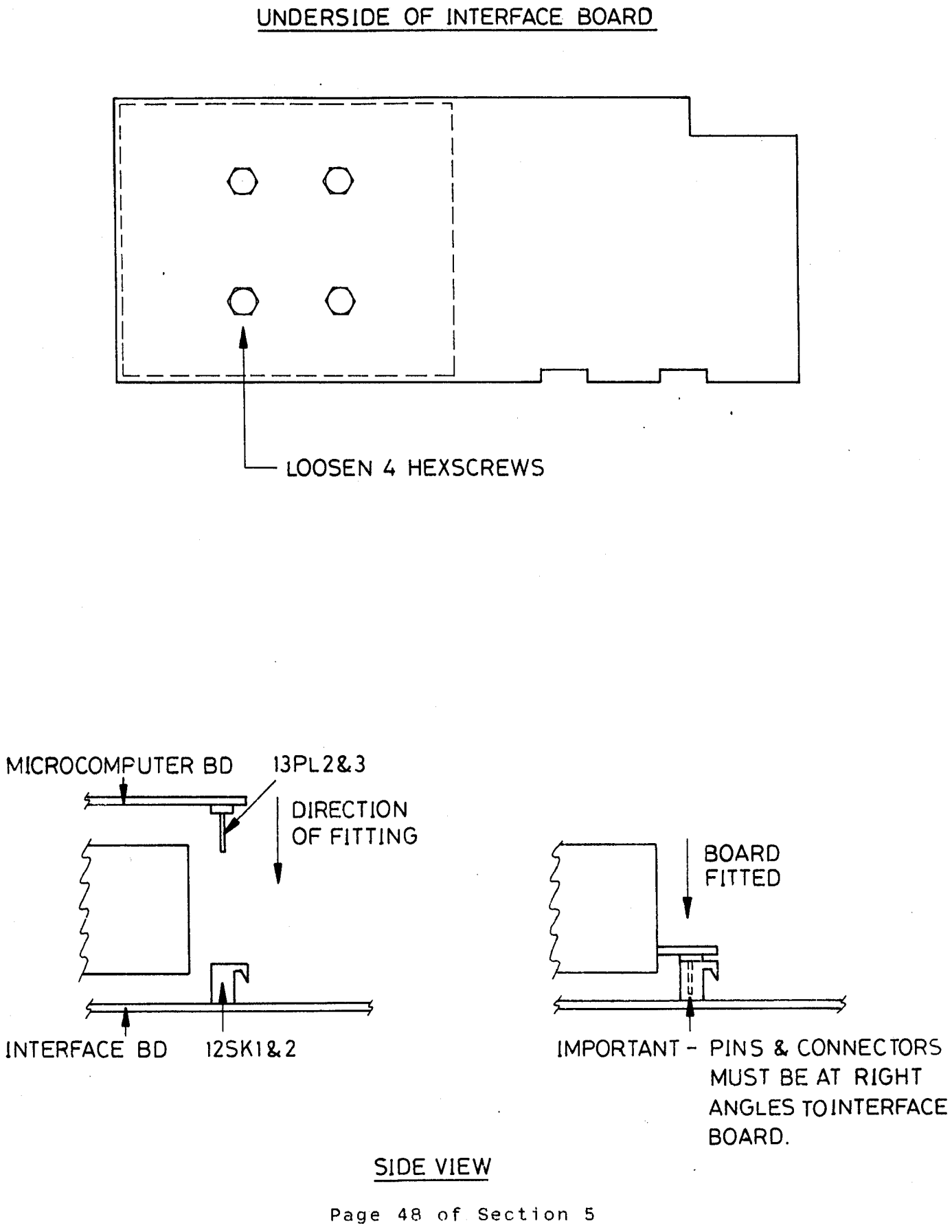
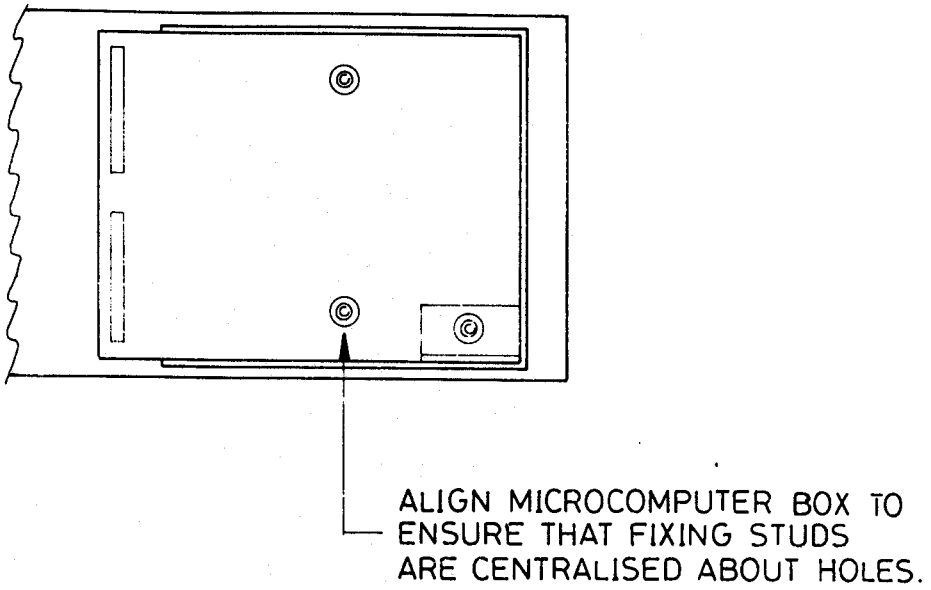


Figure 5.11
Microcomputer Alignment (2)

PLAN VIEW OF MICROCOMPUTER BOARD IN POSITION



UNDERSIDE OF INTERFACE BOARD

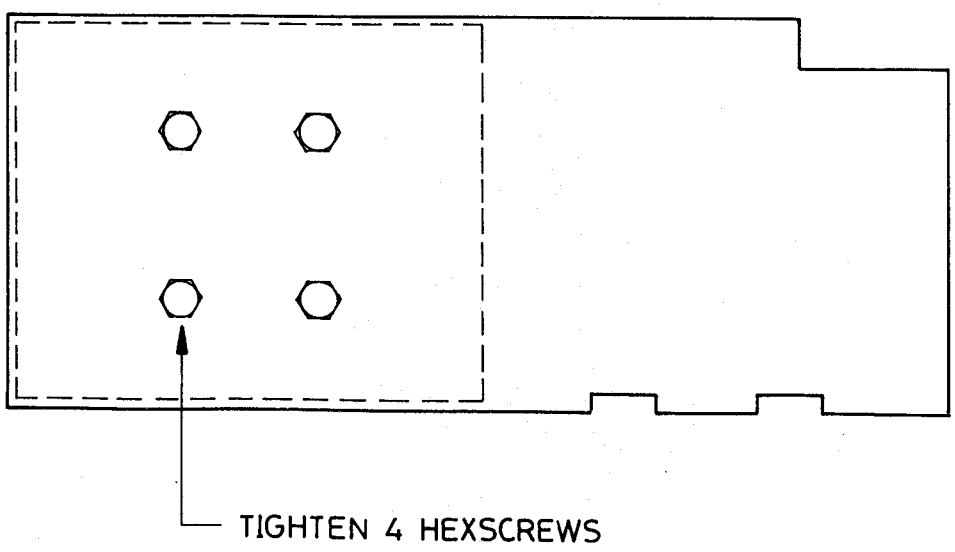
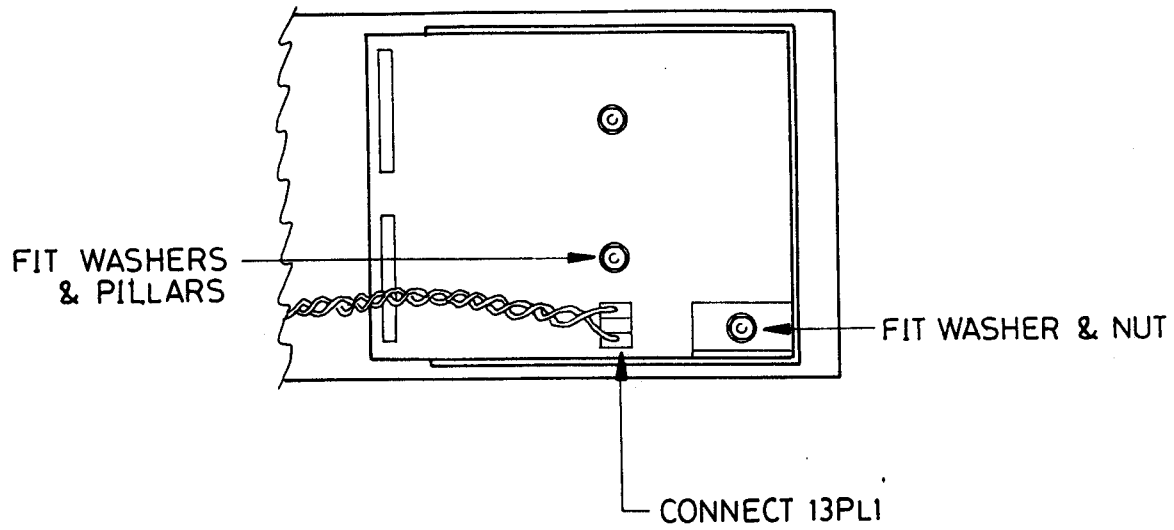


Figure 5.12
Microcomputer Alignment (3)

PLAN VIEW OF MICROCOMPUTER BOARD IN POSITION



5.2.5 DISPLAY BOARD

1) See section 5.2.3.

2) Remove front panel control knobs.

3) Remove connector 11PL3.

3) Remove five M3X8 fixing pillars and washers and three M3X6 hexscrews and washers.

4) Withdraw display board from studs.

N.B. Take care not to lay the display board on it's LED face in order to avoid damage to the latter.

5.2.6 POWER SUPPLY BOARD

1) Remove top and bottom dust covers.

2) Disconnect all leads from the power supply board.

3) Remove five M4 fixing screws and washers which 'sandwich' rear panel between the power supply heatsinks.

4) Ease finned heatsink assembly from rear panel and carefully ease out power supply board and heatsink bracket through the top of the receiver.

Re-assembly

Re-assembly is the reverse of the above. However, it is important that all 'heatsink compound' is replaced with new (Dow Corning DC340) and similarly any damaged insulating items.

5.2.7 MAIN IF AND AUDIO BOARD

1) Remove top and bottom dust covers.

2) Disconnect all connectors from the main IF and audio board removing covers over board sections as required.

3) Remove ten M3X6 and one M3X8 fixing screws and washers.

N.B. The M3X8 fixing screw has an M3 overlapping tooth washer associated with it. This ensures proper 'single point earthing ' of the audio stage and must be replaced in the same position i.e. fixing adjacent to 10PL7.

4) Withdraw main IF and audio board upwards clearing leads and noting position of cable harness underneath.

Re-assembly

Re-assembly is the reverse of the above. However, it is important that all pillars are tightened before the printed circuit board is replaced in the chassis and that subsequently no leads are trapped .

5.2.8 1st IF BOARD

1) Remove top and bottom dust covers.

2) Disconnect all connectors from the RF and 1st IF board removing covers over board sections as required.

3) Remove ten M3X6 fixing screws and washers.

4) Withdraw 1st IF board upwards clearing leads and chassis.

Re-assembly

Re-assembly is the reverse of the above. However, it is important that all pillars are tightened before the printed circuit board is replaced in the chassis and that subsequently no leads are trapped.

5.2.9 RF AMPLIFIER BOARD

1) Remove top and bottom dust covers.

2) Disconnect all connectors from the RF amplifier board removing covers over board sections as required.

3) Remove four M3X6 fixing screws and washers

4) Withdraw RF amplifier board upwards clearing leads and chassis.

Re-assembly

Re-assembly is the reverse of the above. However, it is important that all pillars are tightened before the printed circuit board is replaced in the chassis and that subsequently no leads are trapped.

5.2.10 SYNTHESISER BOARD

1) Remove top and bottom dust covers.

2) Remove synthesiser cover and note position of any earth straps removed.

3) Disconnect all connectors from the synthesiser board removing covers over board sections as required. Extract ribbon cable connector from interface board 12RS3 and note lead positions.

4) Remove six M3X6 fixing screws, four M3X20 pillar/studs and associated washers.

5) Withdraw synthesiser board upwards clear of synthesiser box. Take care not to disturb leads in close proximity to the VCO box.

Re-assembly

Re-assembly is the reverse of the above. However, it is important that all pillars are tightened before the printed circuit board is replaced in the chassis and that subsequently no leads are trapped.

N.B. Where the 'first loop' below board screen has been disturbed it must be re-aligned before the synthesiser board is replaced.

6) Refering to Figure 5.13/14 remove below board screen.

7) Loosen four M3X6 screws in screen allowing earthing bars to 'float'.

8) Re-assemble four pillar/studs and 'first loop' cover and then tighten earthing bars in the attitude adopted.

9) Disassemble four pillar/studs and 'first loop' cover and refit below board screen to synthesiser box.

10) Replace synthesiser board.

Figure 5.13
Synthesiser 'Below Board' Screen Alignment (1)

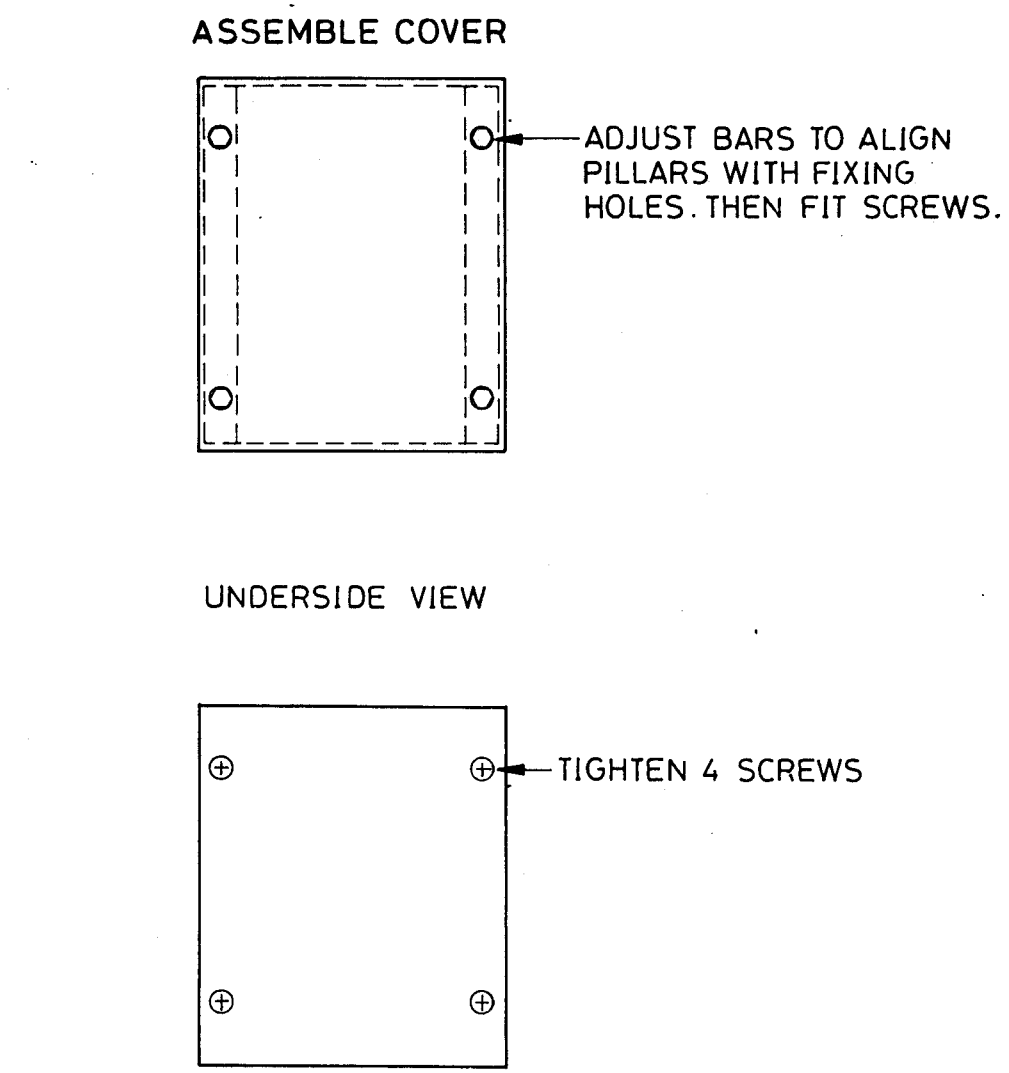
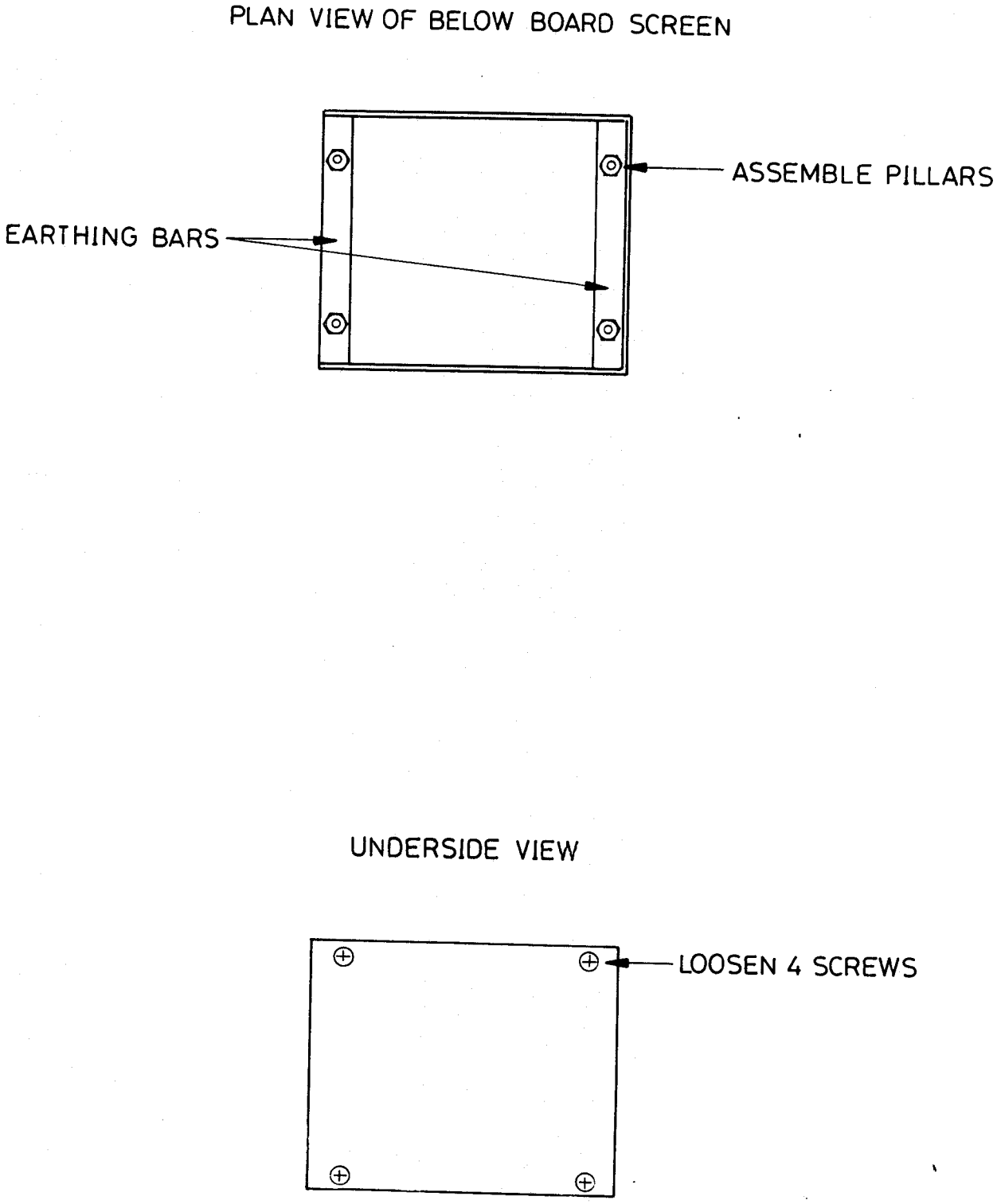


Figure 5.14
Synthesiser 'Below Board' Screen Alignment (2)



5.2.11 VCO MODULE

1) Remove top and bottom dust covers.

2) Remove synthesiser cover and note position of any earth straps removed.

3) Remove VCO cover and note position of any earth straps removed.

4) Disconnect all leads from the VCO board removing the adhesive as necessary.

5) Remove five M3X6 fixing screws and washers.

6) Remove VCO board.

N.B. An access hole is provided to allow removal of the synthesiser box obviating the need to remove the VCO box.

The VCO box is supported on flexible mounts insulating the former both mechanically. and electrically.

7) Remove four slotted head screws saving eight bushes and withdraw VCO box.

Re-assembly

Re-assembly is the reverse of the above. The flexible mounts should be firm but not distorted. All leads should be re-positioned and adhesive applied as Figure 5.2.

5.2.12 PRE-SELECTOR MODULE

1) Remove top and bottom dust covers.

2) Remove pre-selector cover (four M3X6 screws) taking care to avoid damage to foam pad on underside. Note cable positions.

3) Disconnect 3PL5, 3PL6 and 3PL7. Disconnect ribbon cable at 12RS4 and clear back to pre-selector board.

4) Remove HF coil board reference 4 and remove eight M3X6 retaining screws and clear board upwards from box.

N.B. Relay boards and coil boards may be removed by unplugging them from the main board without removal of the latter.

Re-assembly

Re-assembly is the reverse of the above. Ensure that twisted lead 3PL7 is held by rear board retaining screw cable clip near exit aperture and ensure that co-axial lead 3PL6 is guided through adjacent aperture in module box side. When refitting module box cover, ensure that foam 'relay board retaining pad' is above these boards.

5.2.13 NBFM BOARD

(/N Receivers only)

1) Remove top and bottom dust covers.

2) Remove module cover held by four M3X6 screws and washers.

3) Disconnect both connectors from the NBFM board and clear the wiring.

4) Remove two M3X6 and one M3X20 screws and washers and withdraw PCB.

Re-assembly

Re-assembly is the reverse of the above.

5.2.14 FSK BOARD

(/K Receivers only)

1) Remove top and bottom dust covers.

2) Disconnect both connectors from the FSK board and clear the wiring.

3) Remove two M3X6 and one M3X20 screws and washers and withdraw PCB.

Re-assembly

Re-assembly is the reverse of the above.

5.2.15 EXTERNAL STANDARD BOARD

(/S Receivers only)

1) Remove top and bottom dust covers.

2) Remove synthesiser cover and note position of any earth straps removed.

3) Disconnect three connectors from the External Standard board and clear the wiring.

4) Remove four M3X6 screws and washers from the External Standard board allowing it's detachment from the Synthesiser board.

Re-assembly

Re-assembly is the reverse of the above. It is important that the mounting pillars attached to the Synthesiser board are tightened before the External Standard board is re-fitted and that no wiring is trapped as a result.