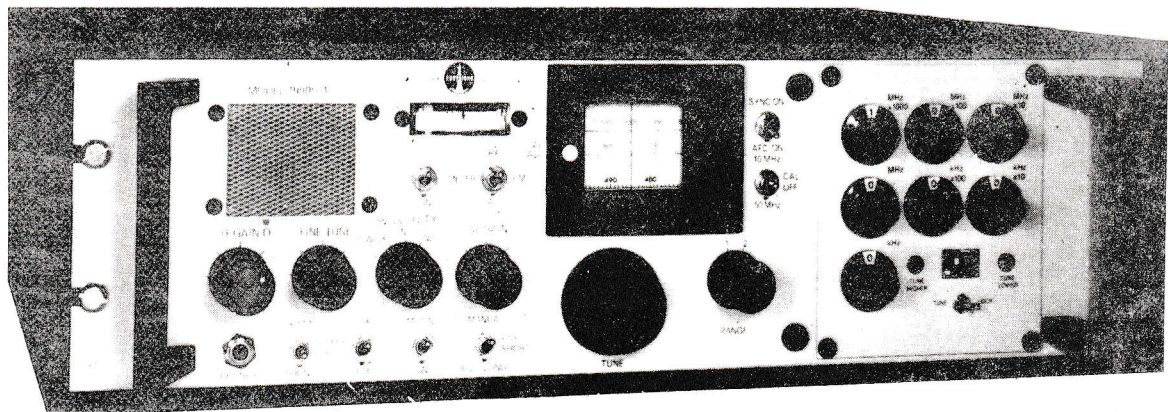


# **Eddystone**

## **DIGITAL SYNCHRONISER**

### **For**

## **MODEL 1990S SERIES**



*Manufactured in England by Marconi Instruments Limited for*



**EDDYSTONE RADIO LIMITED**

MEMBER OF MARCONI COMMUNICATION SYSTEMS LIMITED  
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## AMENDMENT RECORD

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The Manufacturer reserves the right to modify the content of this publication as necessary to accommodate modifications, design improvements etc. Relevant Amendment Sheets will be incorporated at date of issue.

# INTRODUCTION

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## **General**

This manual provides comprehensive instructions for the servicing and maintenance of the frequency synchroniser as used in the Model 1990R suffix "S" receivers. Operating instructions are included in the 1990R receiver handbook, and brief notes are given here for the sake of completeness.

## **Guarantee**

The synchroniser is covered under the same guarantee as the receiver.

## **Servicing**

Spares for user servicing can be supplied and helpful advice will be given freely when required. Any enquiries relating to service matters should be directed to the "Sales and Service Dept." at our usual address.

Should major servicing become necessary, where it has been established that the fault lies in the synchroniser and not in the main part of the receiver, then the synchroniser only may be returned to Eddystone Radio. In other cases the receiver and synchroniser should be returned as a complete unit. The serial number of both receiver and synchroniser should be quoted in all communications and care should be taken to ensure that the equipment is well protected against possible damage during transit.

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## Section 1

# OPERATION

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These notes are included for the sake of completeness only. Full details of operating procedures are given in the Model 1990S Receiver Manual.

### Controls

#### TUNING CONTROL SWITCHES

Seven switches allow the receiver frequency to be set, to increments of 1kHz.

#### TUNE-LOCK SWITCH

In the TUNE position the receiver can be tuned normally. In the LOCK position the Variable Frequency Oscillator in the receiver is locked to the synchroniser.

### Tuning

Two methods of operation will be described:—

When the signal frequency is known precisely:

- (a) Adjust the tuning control switches so that an exact readout of the signal frequency is obtained.
- (b) Tune the receiver to the signal frequency. The direction in which the tuning must go is indicated by the two lamps TUNE HIGHER or TUNE LOWER. The lamps will flash alternately when the setting is correct.
- (c) The TUNE/LOCK switch should now be set to LOCK. The receiver is now locked to the frequency set by the synchroniser.

When the signal frequency is not known precisely:

- (a) Tune the receiver to the desired signal using the TUNE control.
- (b) Set the tuning control switches on the synchroniser to give the same frequency read-out as the receiver tuning scale. Slight adjustment of the least significant knob may be necessary to make the indicator lamps flash alternately. The maximum setting accuracy which may be achieved is +1kHz.
- (c) The TUNE/LOCK switch may now be set to LOCK. The receiver is now locked to the frequency set by the synchroniser.
- (d) If the receiver goes off tune when this is done it is an indication that the synchroniser is not set exactly to the signal frequency and more exact adjustment is required. The meter situated between the tuning lamps gives an indication of the degree of synchronism between the receiver and the synchroniser. With the switch in the LOCK position the pointer will rest at centre scale if the two frequencies are identical.

Use of the synchroniser is recommended when using narrow bandwidth filters in the receiver.

## TECHNICAL DATA & CIRCUIT DESCRIPTION

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### TECHNICAL DATA

#### General Specification

(To be read in conjunction with Model 1990S Receiver Specification).

#### Frequency Coverage

440-1000MHz in increments of 1kHz.

#### Frequency Setting Accuracy

$\pm 1$ kHz.

#### Frequency Stability

5 parts in  $10^8$  /degree C over the range  $-10^{\circ}\text{C}$  to  $+50^{\circ}\text{C}$ .

#### Dimensions and Weight

Panel : 108 x 127mm ( $4\frac{1}{4}$ in. x 5in.)

Weight : 2.27kg (5lb).

#### Power Supplies

All power supplies are derived from the parent receiver.

# CIRCUIT DESCRIPTION

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This description should be read in conjunction with the circuit diagrams found at the rear of this manual, and with the description of the parent receiver. The upper frequency limit is 1000MHz for Model 1990S receiver.

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Solid state circuits are employed throughout to ensure long term reliability and the design provides for easy access to all components for servicing.

If desired, the receiver can be used independently by setting the TUNE-LOCK switch to TUNE.

## PRINCIPLE OF OPERATION

When the synchroniser is used to lock the frequency of the 1990S as shown in the block diagram Fig. 2.1 the configuration is that of a phase locked frequency synthesizer.

Output from the crystal reference oscillator at a frequency  $f_r$  is passed to a series of fixed ratio dividers to produce a reference  $f_r/m$  which is applied to one input of a phase detector.

The RF output signal from the VFO at a frequency  $f_o$  is passed to a series of variable ratio dividers to produce a signal frequency  $f_o/n$  which is applied to the second input of the phase detector.

When the frequency of the oscillator is set so that  $f_o/n$  is correctly related to  $f_r/m$  the control signal from the phase detector will be held constant.

If the frequency of the variable frequency oscillator drifts, the two frequencies will not be correctly related, causing the AFC signal from the phase detector to change in a manner such that the frequency of the receiver will be corrected.

Output from the variable frequency oscillator can be between 47.65MHz and 103.65MHz (due to divider in receiver) and it is first necessary to amplify this signal before prescaling it by a factor of 20 to ensure that it never exceeds the frequency handling capability of the variable ratio divider. When the variable ratio divider is set to display the desired frequency by the switches on the front panel of the synchroniser it has a ratio such that when the receiver is tuned to the set frequency, its output is a train of 5Hz pulses. This signal is passed to a sample and hold type phase detector where it is compared with a 50Hz ramp waveform obtained by dividing and shaping the output of an internal 5MHz crystal controlled oscillator. If the receiver frequency is not precisely that set by the synchroniser a correcting voltage will be produced by the phase detector. This voltage is applied to the synchroniser amplifier circuit where it is converted to the correct phase and level for application to the AFC circuits in the receiver. Correct locking is indicated by the "IN LOCK" meter.



## CIRCUIT DESCRIPTION

### TUNING

When the TUNE-LOCK switch is in the TUNE position, the synchroniser circuit is employed to some extent as a frequency counter. The variable ratio divider then operates to provide 50Hz pulses and these are used as gating signals for a counter consisting of three decade dividers and a flip-flop, whose clock frequency is obtained from the standard divider chain and is 50kHz, see Fig. 2.2. When the frequency entering the synchroniser is higher than that displayed by the dials the gating signal will be at a p.r.f. greater than 50Hz so the counter will be re-set before 1000 pulses have been counted and consequently the final flip-flop will change state. The flip-flop drives a monostable circuit which produces outputs to drive the L.E.D. frequency finding indicators. When operating as described, the TUNE LOWER indicator will be lit. When the frequency entering the synchroniser is lower than that set by the switches the flip-flop will change state at regular intervals, this drives the monostable permanently into its triggered state causing the TUNE HIGHER indicator to be lit.

### Variable Ratio Dividers and Offset Detector

The local oscillator signal from the receiver is divided by the variable ratio divider to give an output frequency of 5Hz for comparison with the crystal standard in the phase detector. The variable ratio divider is complicated by the necessity to display on the frequency selection knobs the signal frequency which differs from the local oscillator frequency by the amount of the receiver I.F.

The counter counts from a number set by the switches to a higher number set by the offset detector. The first number is the 9's complement of the signal frequency, i.e.  $(999\ 999\ 9) - (\text{signal frequency})$ , and the second number is (counters all full) + (receiver I.F.), i.e.  $(999\ 999\ 9) + (003\ 650\ 0)$ . The local oscillator being above the signal frequency the second number is 1 003 649 9 which means that the last stage of the counters can be a simple divide-by-two stage, IC16. The rest of the counting chain consists of presettable divide-by-ten counters, the presetting (in BCD form) is done by the frequency selection switches which are wired so that the 9's complement is set automatically. BCD outputs from the counters are fed into the offset detector.

Notice that each counting stage resets as it becomes full, a feature which considerably increases the speed of operation. A further increase in speed is needed in the TUNE mode when a more rapid response of the TUNE lamps is desirable. This is done by bypassing one of the decade stages, when the output pulse frequency to the phase detector becomes 50Hz.

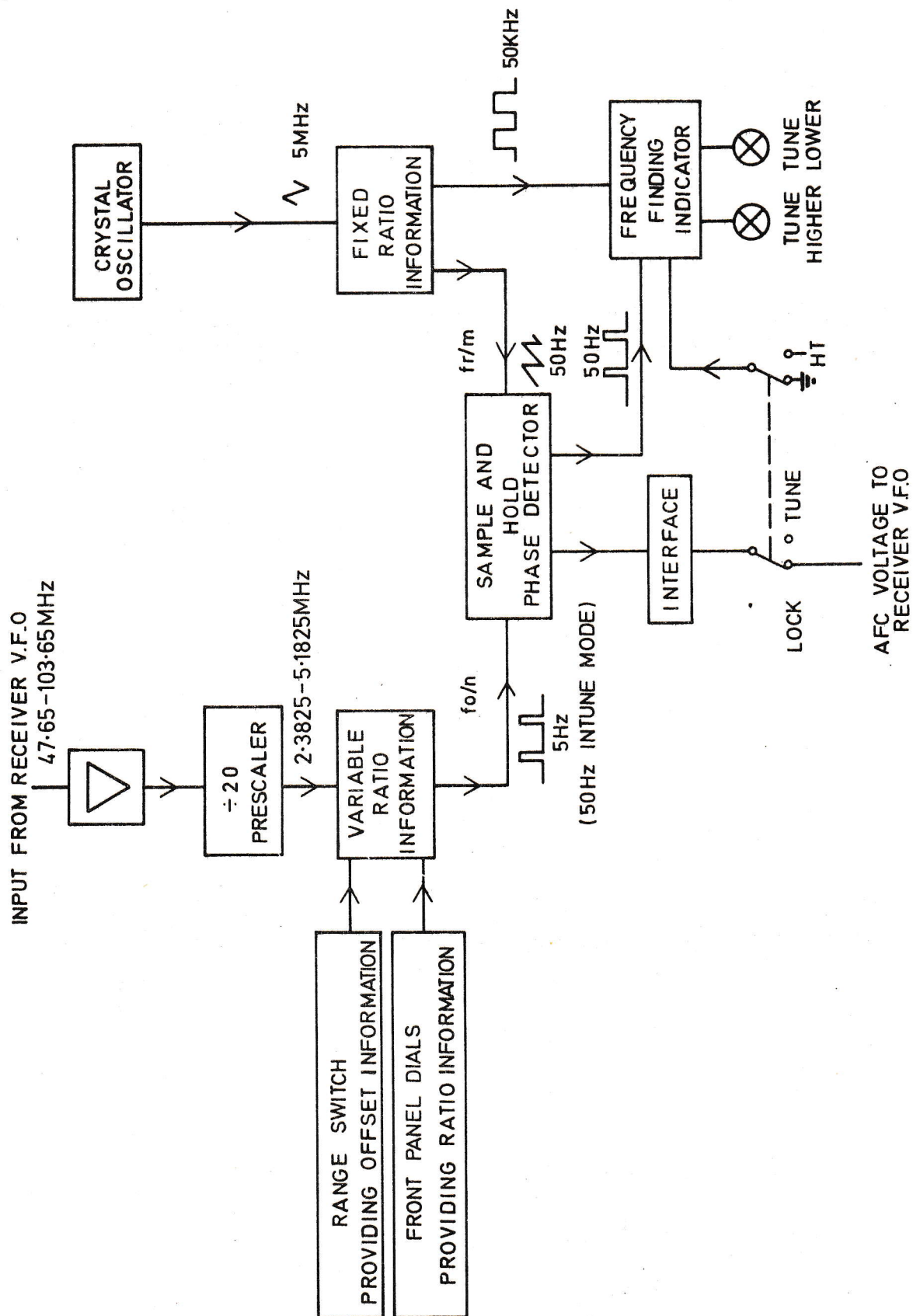


FIG.2.1. FUNCTIONAL DIAGRAM



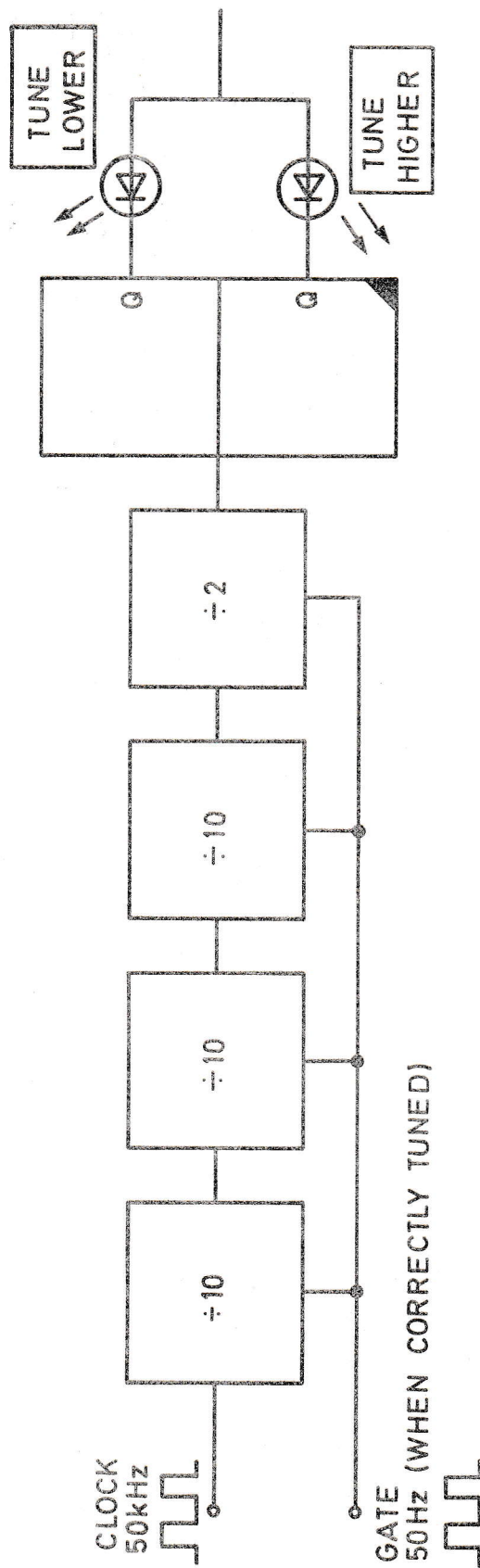


FIG. 2.2. FREQUENCY FINDING INDICATOR FUNCTIONAL DIAGRAM

## MAINTENANCE

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The synchroniser employs semi-conductor devices which although having inherent long term reliability can be damaged by overloads, reverse polarity, and excessive heat or radiation. Care should be exercised to ensure that d.c. supplies are not reversed, avoid prolonged soldering, and strong r.f. fields. Before applying continuity or insulation tests or before shorting or breaking a circuit refer to the circuit diagram to establish the effect on the bias arrangement of the devices employed.

When working on the receiver or synchroniser it will be necessary for power to be connected. It is recommended that the receiver is fed from an isolated power supply and that normal precautions for safety under these conditions are observed.

First Aid notes can be found inside the front cover.

### OVERALL PERFORMANCE TEST

With the 1990S connected to the supply and switched on, correct performance of the synchroniser can be quickly ascertained by performing the following test:

1. Connect a signal generator set to 600MHz to aerial input 1 socket of the 1990S.
2. Set the synchroniser at 600MHz (0 6 0-0 0 0-0) then with the TUNE-LOCK switch at TUNE set the 1990S to 600MHz.
3. Set the TUNE-LOCK switch at LOCK - the pointer of the lock meter should be within the WHITE BOX on the scale.

### PRELIMINARY CHECKS

1. Check to ensure that all switches are undamaged and operating correctly and verify that connectors are securely mated.
2. Check using the multimeter on low ohms range that electrical connections to chassis and earth points have low contact resistance.

## MAINTENANCE

### TEST EQUIPMENT

The use of the following items of test equipment from the list on page 41 of the 1990R Manual is recommended.

Table 3.1

1	Multimeter	(GEC Selectest or Avometer Model 8)
2	Frequency Counter	(Range up to 500MHz 1Hz resolution at 10MHz)
3	H.F. Oscilloscope	(Marconi TF 2210 or equivalent)
4	R.F. Signal Generator	(Marconi TF 2015 or equivalent)

### FAULT FINDING

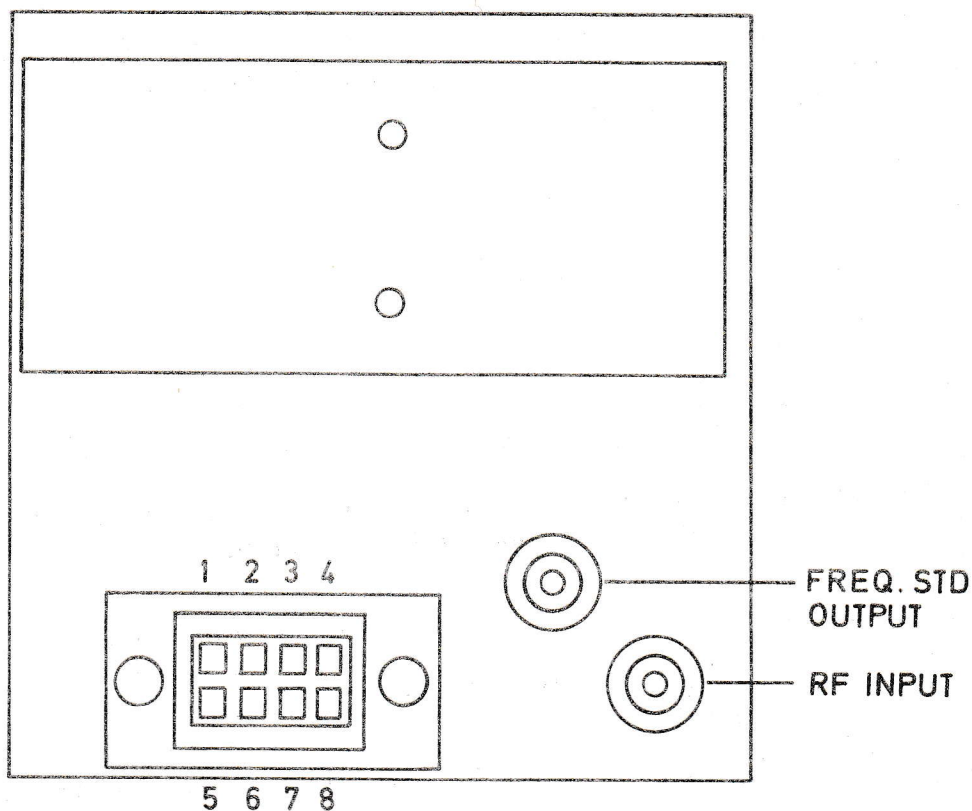


Fig. 3.1 Rear View of Synchroniser

With the synchroniser removed from the receiver and with the synchroniser circuits accessible the cause of incorrect operation can be quickly localized by connecting the assembly to the receiver using connecting cables and then performing the tests given below. The test waveforms may vary slightly from the typical waveforms shown. All waveforms are measured between the point indicated and earth.

#### Access

- 1 Remove the four screws securing the synchroniser to the receiver and withdraw the synchroniser unit.
- 2 Remove the two 6 BA screws which hold the rear panel.
- 3 Carefully pull the rear panel backwards to the extent of the wiring and remove the push-on tags to the circuit board.
- 4 Remove the screw in the centre of the left-hand side of the synchroniser case.

- 5 With the rear panel positioned to one side carefully slide the cover backwards and remove it. Reconnect the wiring removed in step (3) and connect the extension cable to the 8-way sockets in the receiver and on the rear panel of the synchroniser.

## TESTING AND REALIGNMENT

### Input Amplifier (Board A2)

- 1 Connect an r.f. input of 100mV rms at 20MHz to the synchroniser r.f. input.
- 2 Connect the oscilloscope to the junction of R19 and R20. The waveform should be similar to that shown below, if necessary adjust RV2 for amplitude of 850mV.

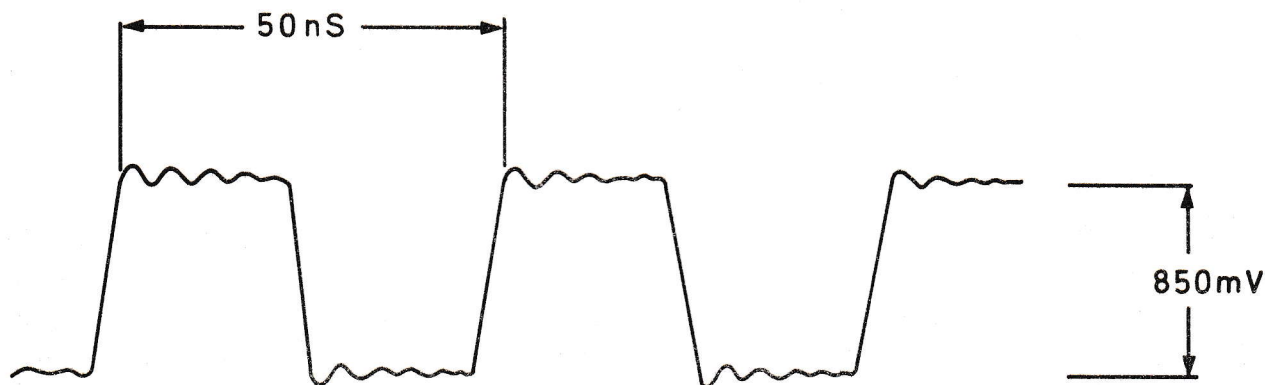


Fig. 3.2

- 3 If an output is not obtained check that the supply voltages are present and check for output signals at the collectors of VT1 and VT2.

### Prescaler

- 1 Connect the oscilloscope to the collector of VT4. The waveform should be similar to that shown below. If necessary adjust RV1 so that the correct frequency is obtained (if more than one setting gives the correct frequency, use the one nearest the centre of the range).

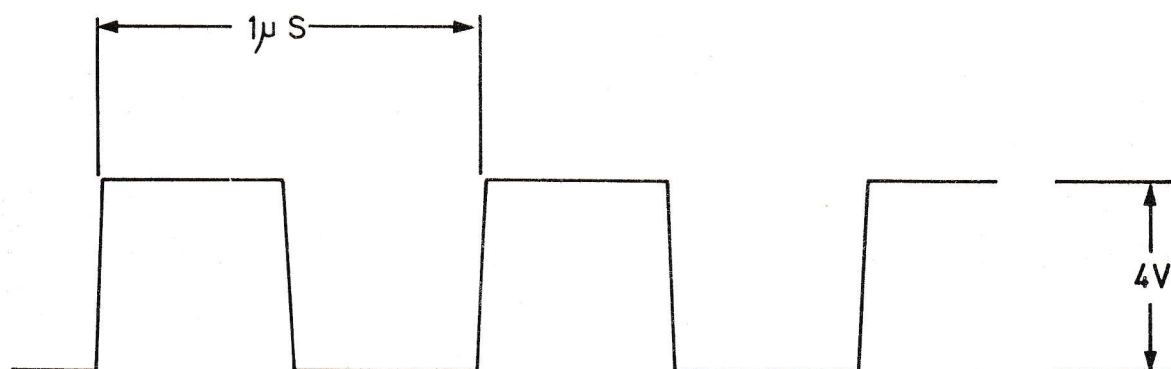


Fig. 3.3

If no output is obtained check for signals at IC2 pin 13 and junction of R11 and R12.



## Variable Ratio Divider and Offset Detector (Boards A2 and A3)

- 1 Set the r.f. input to 100mV at 40MHz, the frequency selection switches to 0 0 3-6 0 0-0, the TUNE-LOCK switch to TUNE, and the receiver to range 1. Connect the oscilloscope to pin 33 on the printed circuit board. The waveform should be similar to that shown below.

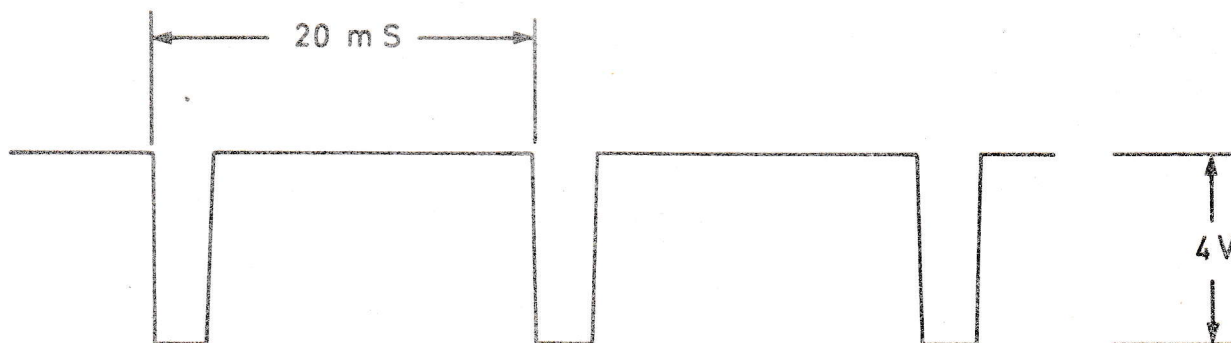


Fig. 3.4

- 2 Check that the waveform is the same for the receiver on ranges 2, 3, 4, 6 and 7.
- 3 Set the r.f. input to 100mV at 20MHz, frequency selection switches to 0 2 0-0 0 0-0 and the TUNE-LOCK switch to LOCK. Connect the oscilloscope to IC7 pin 8. The waveform should be similar to (A) below. Set the TUNE-LOCK switch to TUNE, the waveform should be similar to (B) below.

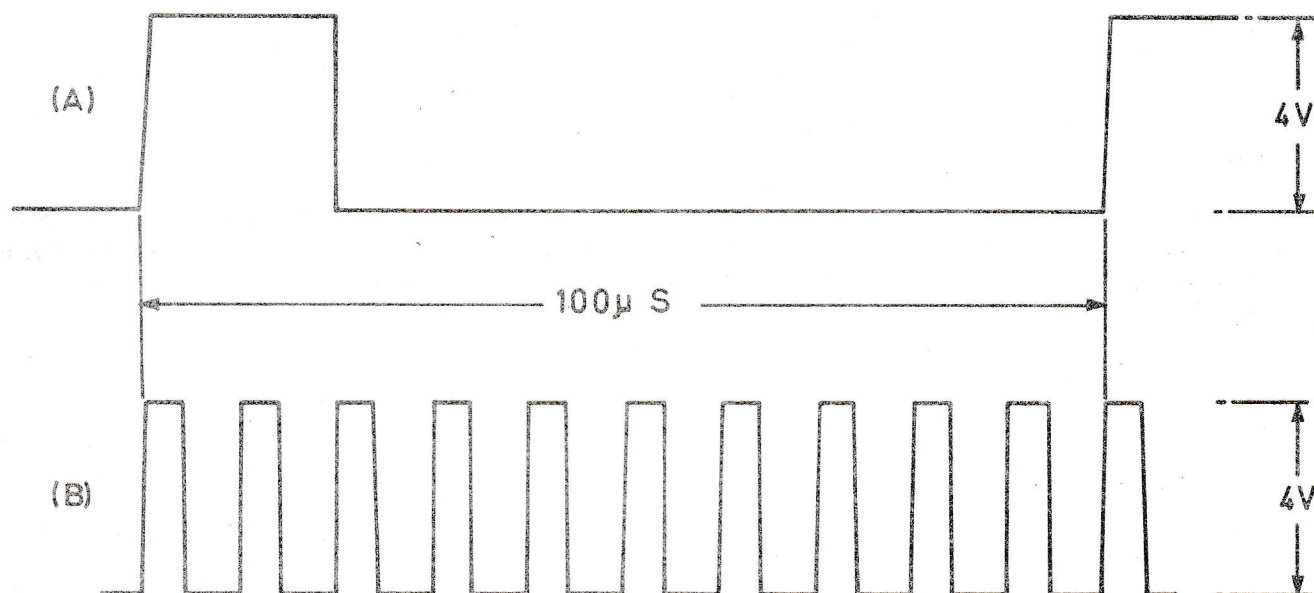


Fig. 3.5 (a) above (b) below

## Standard Divider, Ramp Generator, Sample and Hold Circuits (Board A5)

Set the r.f. input to 100mV at 23.65MHz, frequency selection switches to 0 2 0-0 0 0-0, the TUNE-LOCK switch to TUNE and the receiver to range 1.



- 1 Connect the counter to the 5MHz output on the rear panel and check that the measured frequency is  $5.0\text{MHz} \pm 0.5\text{Hz}$ . Adjust RV1 if necessary to obtain this frequency.
- 2 Connect the oscilloscope to IC1 pin 1. The waveform should be similar to that shown below.

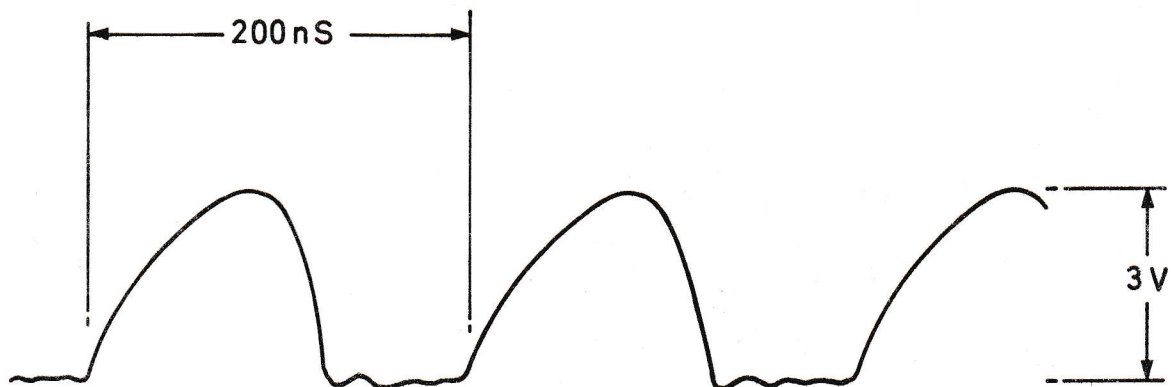


Fig. 3.6

- 3 Connect the oscilloscope to TP1. The waveform should be similar to that shown below. If it is not present check for signal outputs at IC1 pin 12, IC2 pin 12, IC4 pin 12, IC7 pin 11 and IC9 pin 11.

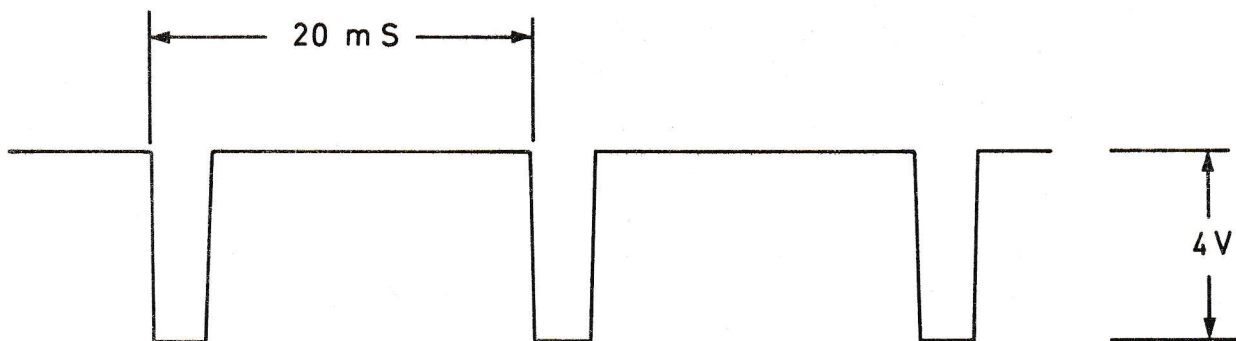


Fig. 3.7

- 4 Connect the oscilloscope to TP2 for the waveform below.

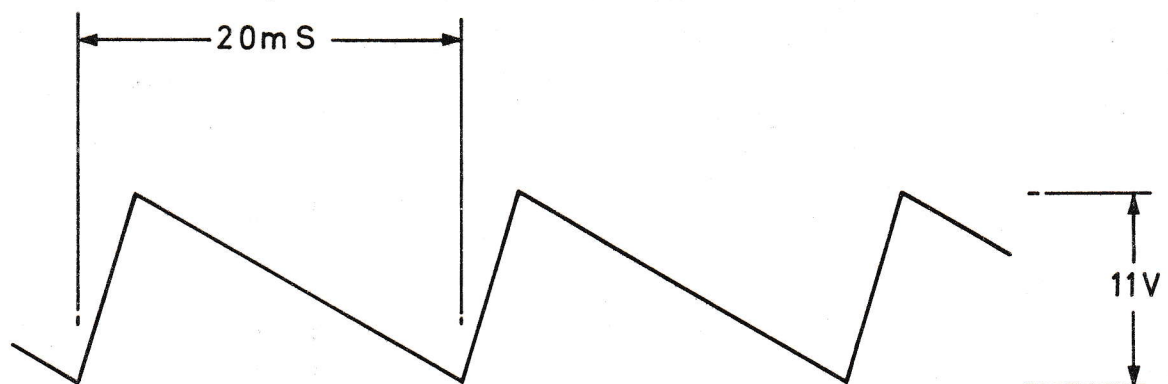


Fig. 3.8

## MAINTENANCE

- 5 Connect the oscilloscope to VT7 source for the waveform below.

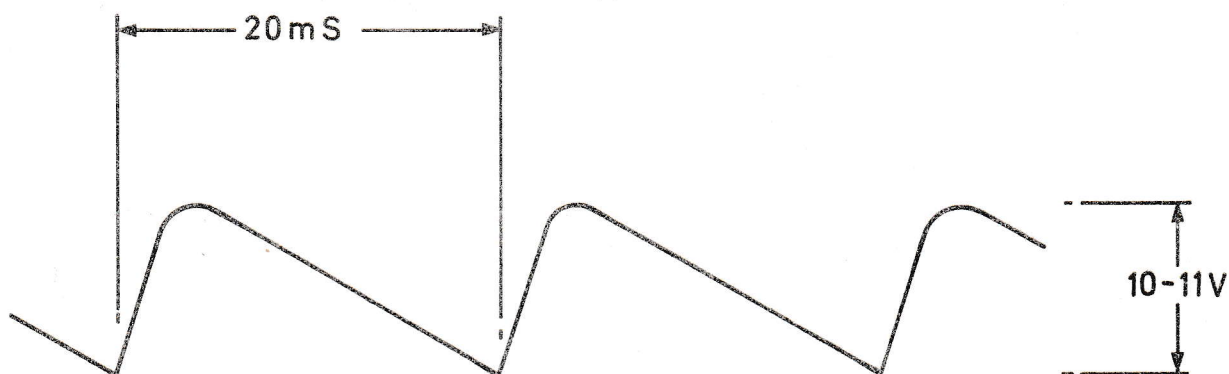


Fig. 3.9

- 6 Connect the oscilloscope to VT4 collector for the waveform below.

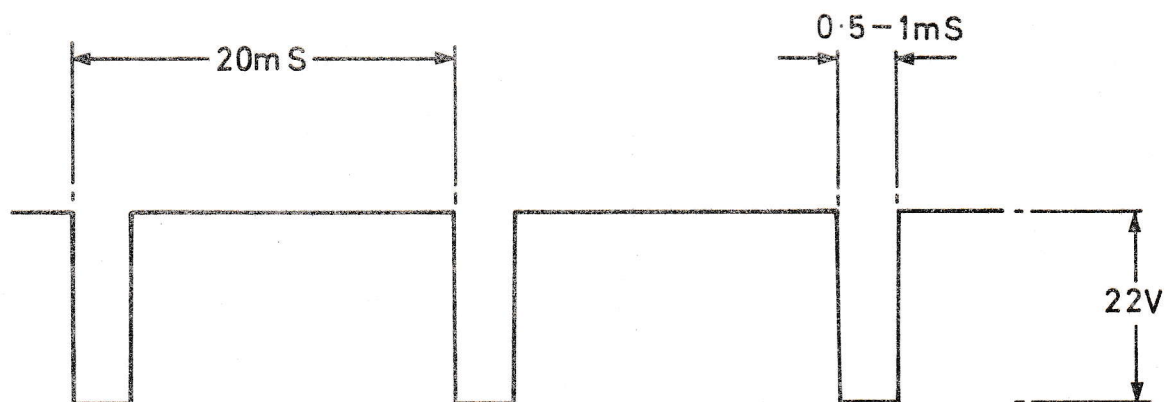


Fig. 3.10

- 7 Connect the oscilloscope to VT6 collector for the waveform below.

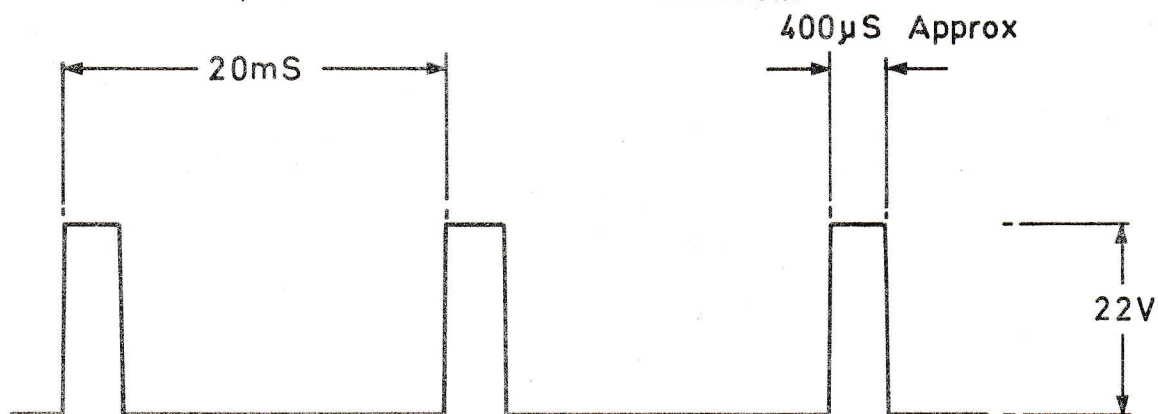


Fig. 3.11

- 8 Connect the oscilloscope to IC3 pin 14 for the waveform below.

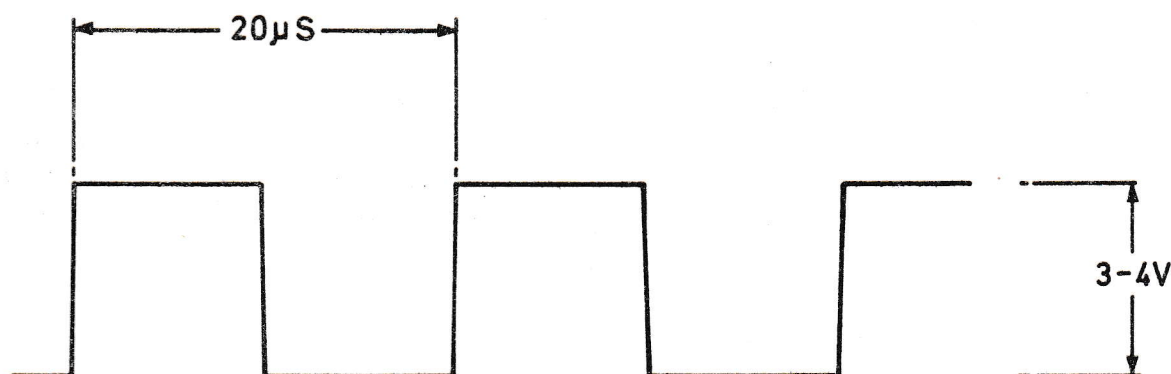


Fig. 3.12

### L.E.D. Circuits (Board A5)

- 1 Set the r.f. input to 100mV at 23.65MHz, the frequency selection switches to 0 2 0-0 0 0-0 the TUNE-LOCK switch to TUNE and the receiver to range 1.

Connect the oscilloscope to IC3 pin 2 and check that the waveform is similar to that shown below.

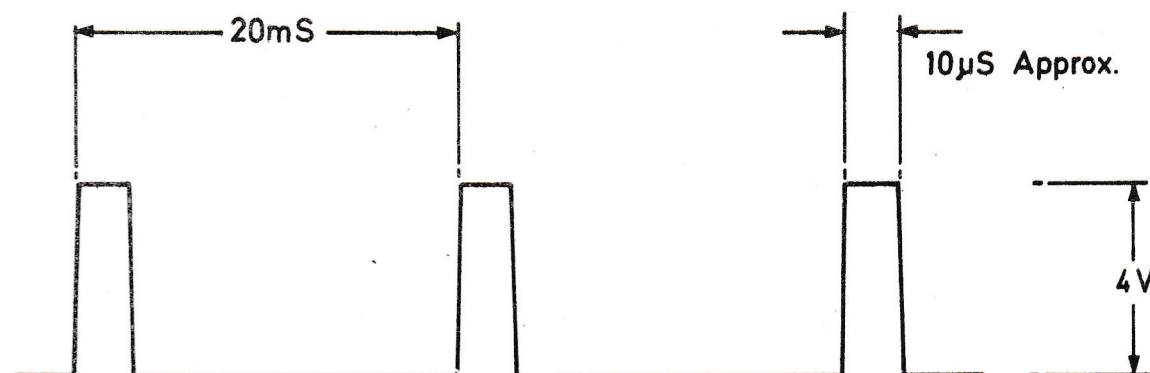


Fig. 3.13

- 2 Connect the oscilloscope to IC13 pin 3 for the waveform below.

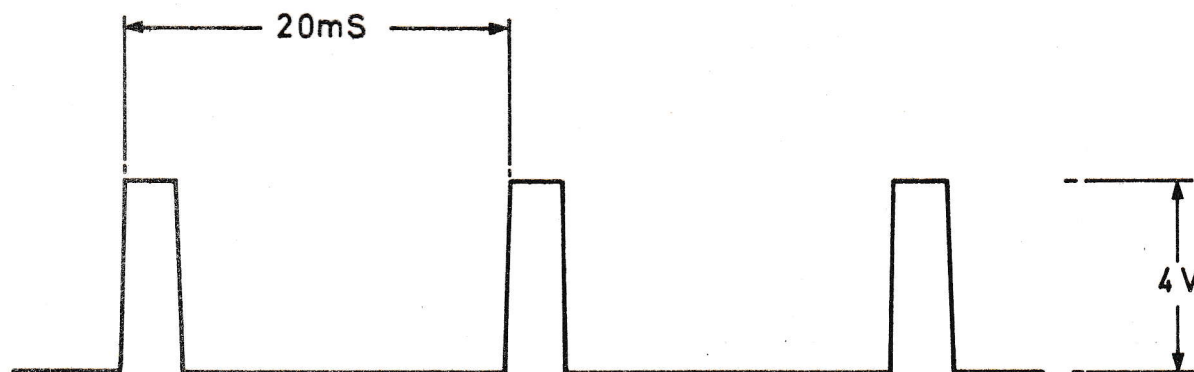


Fig. 3.14

- 3 Connect the oscilloscope (d.c. coupled) to IC13 pin 8.

Set the r.f. input to 40MHz, the voltage should be nominally +5V.  
Set the r.f. input to 42MHz, the voltage should be nominally 0V.

## MAINTENANCE

### Meter Circuits (Board A4)

Set the r.f. input to 100mV at 23.65MHz, the frequency selection switches to 0 2 0-0 0 0-0 and the receiver to range 1. With the TUNE-LOCK switch set to TUNE the two lamps should be flashing. Set the switch to LOCK and allow locking to occur. Adjust RV1 if necessary so that the meter pointer lies in the centre of the white block on the scale. Board A4 is located behind the front panel adjacent to the meter.

# APPENDIX A

## LIST OF COMPONENTS

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Each of the printed circuit boards is allocated a reference number, which is marked on each board. Miscellaneous components are allocated the reference A1. This reference number forms the prefix of the component circuit reference, which should always be quoted in full when ordering spares, but for brevity it is omitted on the circuit diagram and on the printed circuit board legend, where there is no risk of ambiguity.

All orders and enquiries should be directed to the address below, quoting: Type, No. of Receiver, Serial No. of Receiver and Serial No. of Synchroniser in all communications.

EDDYSTONE RADIO LIMITED,  
SALES & SERVICE DEPT.,  
ALVECHURCH ROAD,  
BIRMINGHAM,  
B31 3PP  
ENGLAND

TELEPHONE: 021-475-2231

TELEX: 337081

CABLES: EDDYSTONE BIRMINGHAM

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### CIRCUIT REFERENCE PREFIXES:

A1	Miscellaneous
A2	Variable Ratio Divider Board
A3	Offset Detector Board
A4	Meter Drive Board
A5	Standard Divider Board



# APPENDIX A

## Capacitors

Ref.	Value	Type	Tolerance	Wkg. Voltage
A1C1— A1C21	0.001 $\mu$ F	Ceramic Lead-through	+80%—20%	300V
A1C22	0.47 $\mu$ F	Plastic Film	5%	160V
A1C23	0.47 $\mu$ F	Plastic Film	5%	160V
A1C24— A1C26	0.001 $\mu$ F	Ceramic Lead-through	+80%—20%	300V
A2C1	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C2	10pF	Ceramic	20%	500V
A2C3	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C4	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C5	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C6	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C7	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C8	6.8pF	Ceramic	$\pm 0.5$ pF	500V
A2C9	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C10	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C11	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C12	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C13	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C14	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C15	8.2pF	Ceramic	$\pm 0.5$ pF	500V
A2C16	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C17	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C18	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C19	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C20	82pF	Ceramic	$\pm 10\%$	500V
A2C21	6.8pF	Ceramic	$\pm 0.5$ pF	500V
A2C22	0.22 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A2C23	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C24	0.001 $\mu$ F	Ceramic	+80%—20%	500V
A2C25	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C26	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C27	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A2C28	4.7 $\mu$ F	Electrolytic	+100%—20%	63V
A2C29— A2C37	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A3C1— A3C6	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C1— A5C11	0.01 $\mu$ F	Ceramic	+80%—20%	100V

Ref.	Value	Type	Tolerance	Wkg. Voltage
A5C12	0.47 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C13	0.47 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C14	0.047 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C15	100 $\mu$ F	Electrolytic	+100%—20%	25V
A5C16	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C17	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C18	47 $\mu$ F	Electrolytic	+100%—20%	25V
A5C19	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C20	2.2 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C21	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C22	3.3nF	Plastic Film	$\pm 10\%$	63V
A5C23	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C24	33nF	Plastic Film	$\pm 10\%$	250V
A5C25	0.01 $\mu$ F	Ceramic	+80%—20%	100V
A5C26	0.1 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C27	0.68 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C28	0.22 $\mu$ F	Plastic Film	$\pm 10\%$	63V
A5C29	1000 $\mu$ F	Electrolytic	100%—20%	10V
A5C30	0.01 $\mu$ F	Ceramic	+80%—20%	100V

Ref.	Value OHMS	Ref.	Value OHMS	Ref.	Value OHMS	Ref.	Value OHMS
A1R1	200	A2R17	150	A4R2	5.6k	A5R16	100
A1R2	820	A2R18	220*	A4R3	4.7k	A5R17	22k
		A2R19	68	A4R4	12k	A5R18	47k
		A2R20	620			A5R19	15k
A2R1	39	A2R21	6.8k			A5R20	560k
A2R2	24k	A2R22	240	A5R1	2.2k	A5R21	3.3k
A2R3	240	A2R23	1k	A5R2	2.2k	A5R22	2.2k
A2R4	680	A2R24	430*	A5R3	3.3k	A5R23	180
A2R5	150	A2R25—	10k	A5R4	100k	A5R24	51
A2R6	91	A2R52		A5R5	5.6k AOT		
A2R7	24k	A2R53	560*	A5R6	1k		
A2R8	240	A2R54	2.2	A5R7	22k		
A2R9	680			A5R8	3.3k		
A2R10	150	All A2 & A2		A5R9	120		
A2R11	390*	resistors are 2% ¼		A5R10	47k		
A2R12	3.3k	Watt metal film,		A5R11	6.8k		
A2R13	91	except those marked		A5R12	15k		
A2R14	24k	* which are 2% ½		A5R13	560k		
A2R15	240	Watt metal oxide.		A5R14	22k		
A2R16	680			A5R15	100		
		A4R1	10k				

## APPENDIX A

### Variable Resistors

Ref.	Type
A2RV1	1k $\Omega$ Carbon preset $\pm 20\%$ $\frac{1}{4}W$
A2RV2	100 $\Omega$ Carbon preset $\pm 20\%$ 0.2W
A4RV1	10k $\Omega$ Carbon preset $\pm 20\%$ $\frac{1}{4}W$
A5RV1	2.2k $\Omega$ Carbon preset $\pm 20\%$ $\frac{1}{4}W$
A5RV2	3.3k $\Omega$ Carbon preset $\pm 20\%$ $\frac{1}{4}W$

### Chokes

Ref.	Type
A1L1— A1L16	18 $\mu$ H Filter Coil, Part No. 44247-012

### Diodes

Ref.	Type
A1MR1	FLV116 L.E.D.
A1MR2	FLV116 L.E.D.
A2MR1	MBD102
A2MR2	MBD102
A2MR3	1S6006A
A5MR1	1N4148
A5MR2	HP5082-2835

### Transistors

Ref.	Type
A2VT1	BFY90
A2VT2	BFY90
A2VT3	BFY90



## Transistors (Cont.)

Ref.	Type
A2VT4	2N709
A2VT5	BC107
A5VT1	BF244B
A5VT2	BCY71
A5VT3	BC107
A5VT4	BC107
A5VT5	BF244B
A5VT6	BC107
A5VT7	BF244B
A5VT8	BF244B
A5VT9	BCY71

## Integrated Circuits

Ref.	Type
A1IC1	$\mu$ A7812
A2IC1	SP630B
A2IC2	MC1027P
A2IC3	SN74H00N
A2IC4	SN74H11N
A2IC5—	N8290A
A2IC11	
A2IC12	SN74H102N
A2IC13	SN74H102N
A2IC14	SN74H00N
A2IC15	SN74H00N
A2IC16	SN7472N
A3IC1	SN74H04N
A3IC2	SN74H30N
A3IC3	SN74H04N
A3IC4	SN74H30N
A3IC5	SN74H04N
A3IC6	SN74H30N
A5IC1—	
A5IC5	SN7490N
A5IC6	TT $\mu$ L9601

## APPENDIX A

### Integrated Circuits (Cont.)

Ref.	Type
A5IC7—	SN7490N
A5IC10	
A5IC11	SN7420N
A5IC12—	
A5IC15	TT <sub>μ</sub> L9601

### Miscellaneous

Ref.	Type
A1 M1	Tune Meter 100 <sub>μ</sub> A-0-100 <sub>μ</sub> A
A1 SA	Frequency Selection Switch Hz x 100 4p 10W
A1 SB	Frequency Selection Switch kHz x 1 4p 10W
A1 SC	Frequency Selection Switch kHz x 10 4p 10W
A1 SD	Frequency Selection Switch kHz x 100 4p 10W
A1 SE	Frequency Selection Switch MHz x 1 4p 10W
A1 SF	Frequency Selection Switch MHz x 10 4p 10W
A1 SG	Frequency Selection Switch MHz x 100 4p 10W
A1 SH	Tune-Lock Switch 2p 2W
A5 X1	5MHz Crystal Oscillator Unit QC1311/A
—	Switch Control Knobs comprising: Knob body, Elma 70-14-14 Black Cap, Elma 1450-14 Black Figure Dial, Elma 1452-14/1 Stator, Elma 1453-14/1
A2	Variable Divider Board, Part No. 44827-261
A3	Offset Detector Board, Part No. 44827-262
A4	Meter Drive Board, Part No. 44827-287
A5	Standard Divider Board, Part No. 44827-315
—	Meter Shunt Board, Part No. 44559-015  8-way plug BNC plug-fixed Ribbon Cable

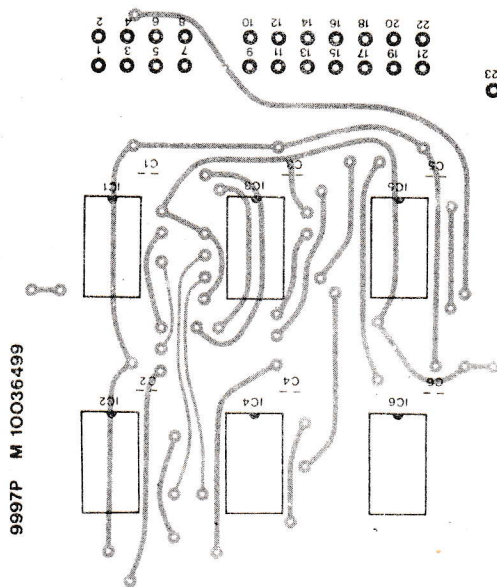


# APPENDIX B

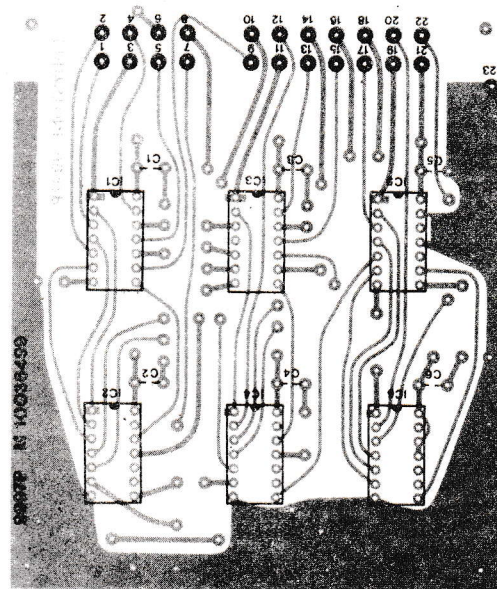
## CIRCUIT DATA

All printed circuit boards are shown viewed from the legend side, i.e. the front face. Double sided boards are shown twice, firstly with the front copper track and legend superimposed, and secondly with the rear copper track (as seen through the laminate) and legend superimposed.

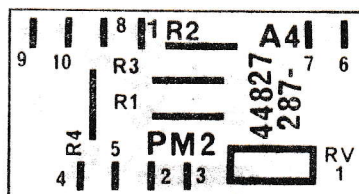
The two divider boards and the offset detector board are double sided and are shown slightly less than actual size, whilst the meter drive board which is single sided is shown enlarged. The meter shunt board carries two resistors only and is not shown.



**OFFSET DETECTOR BOARD**  
showing front copper track

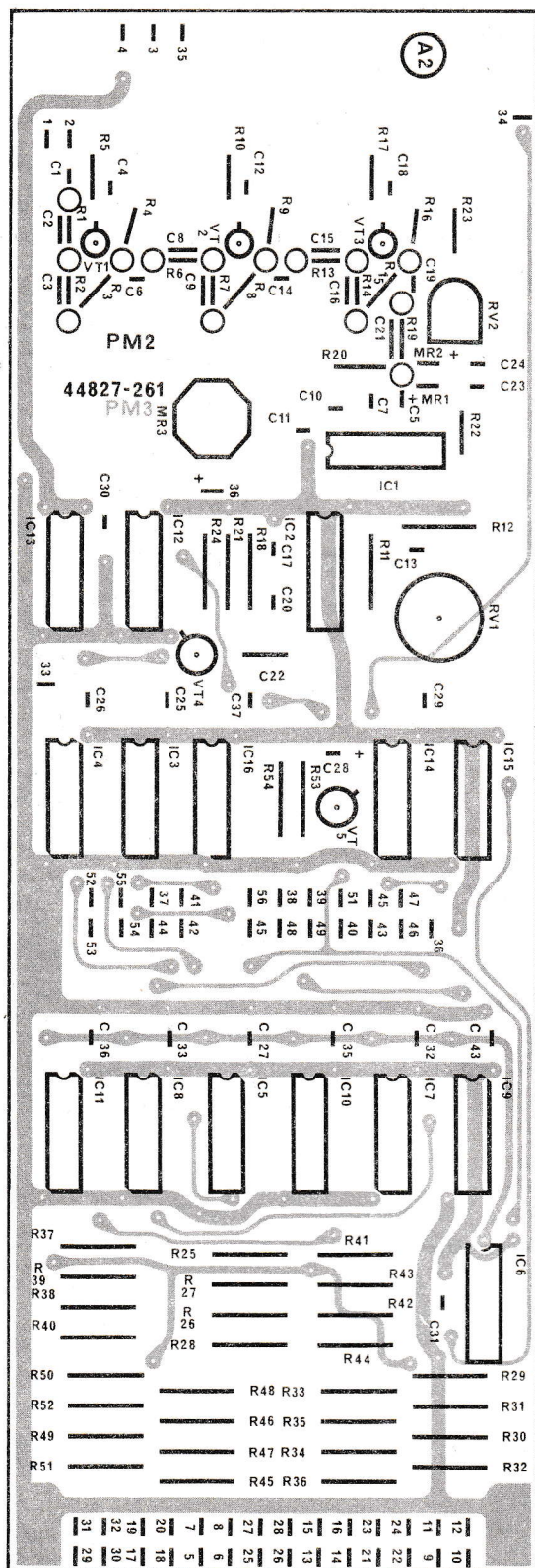


**OFFSET DETECTOR BOARD**  
showing rear copper track

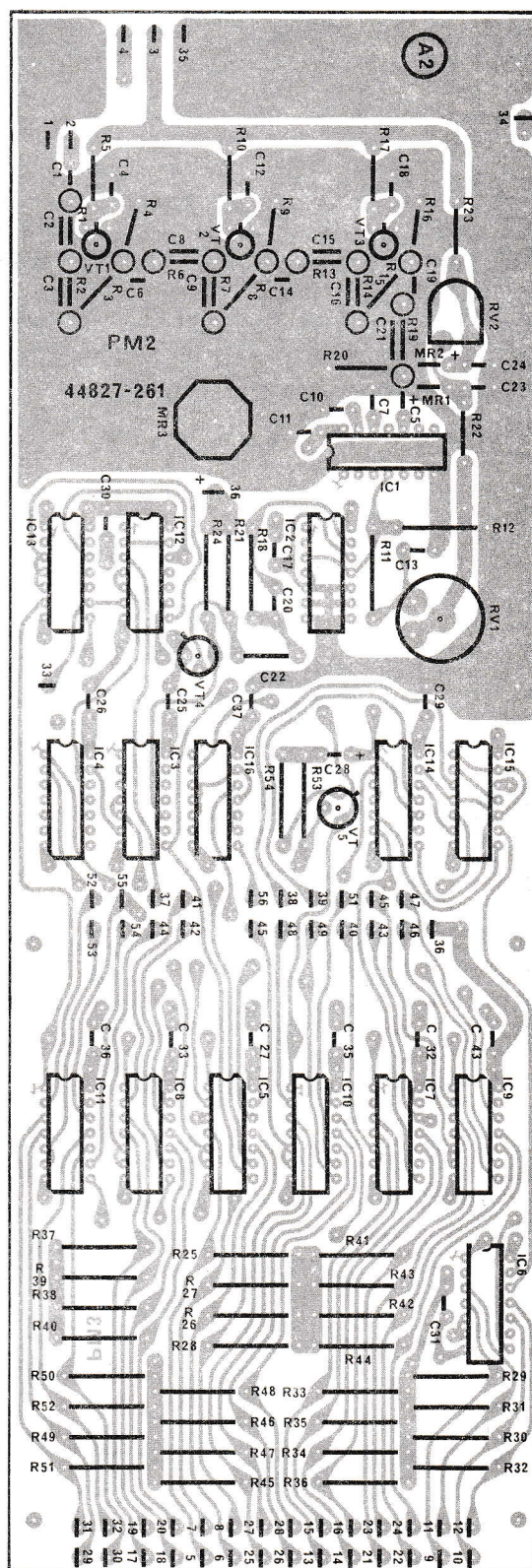


**METER DRIVE BOARD**  
showing rear copper track



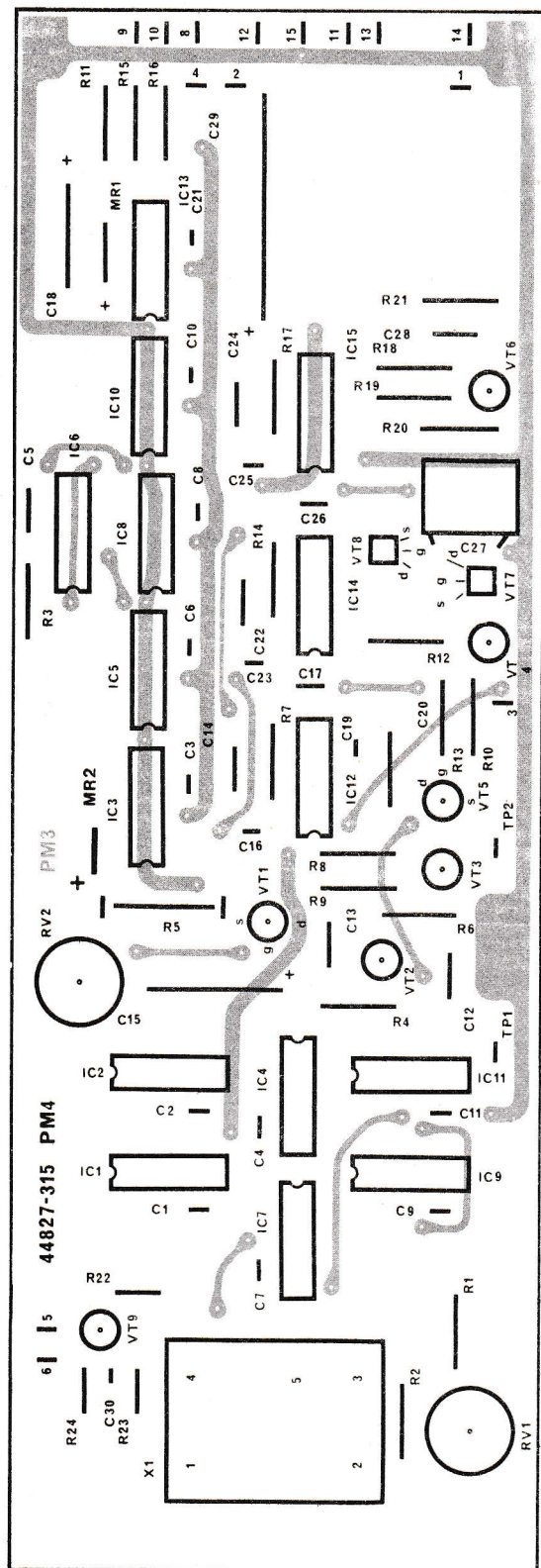


VARIABLE RATIO DIVIDER BOARD  
showing front copper track

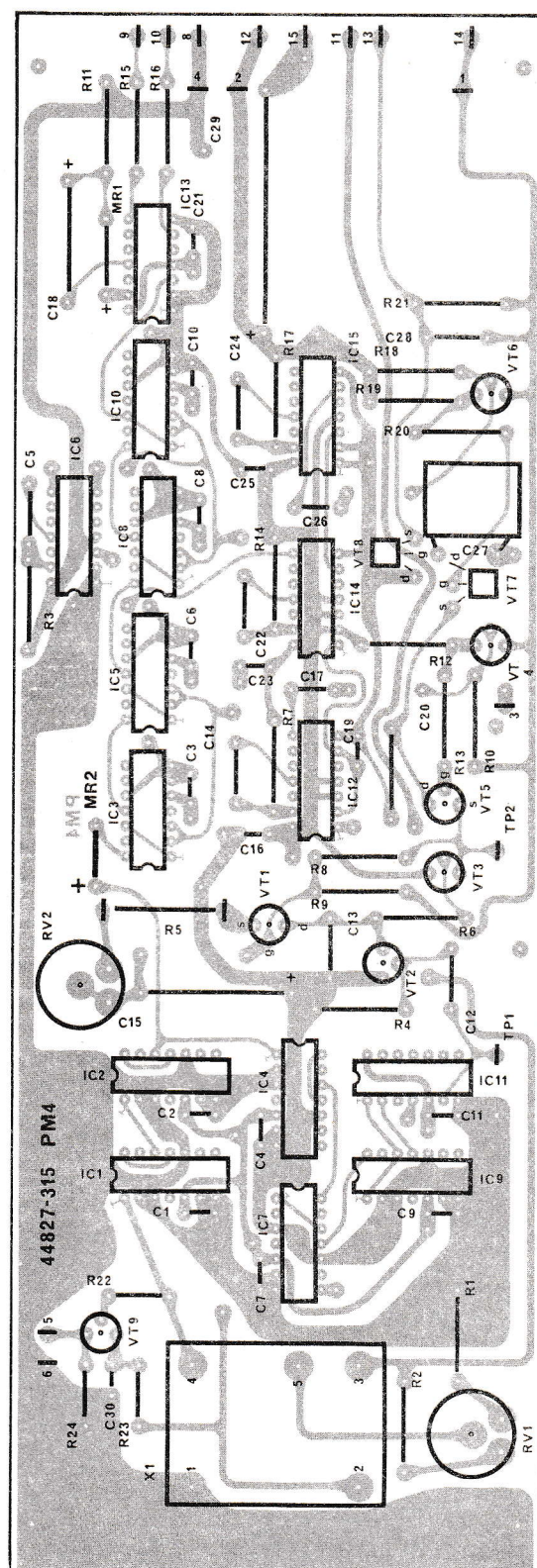


VARIABLE RATIO DIVIDER BOARD  
showing rear copper track





STANDARD DIVIDER BOARD  
showing front copper track



STANDARD DIVIDER BOARD  
showing rear copper track

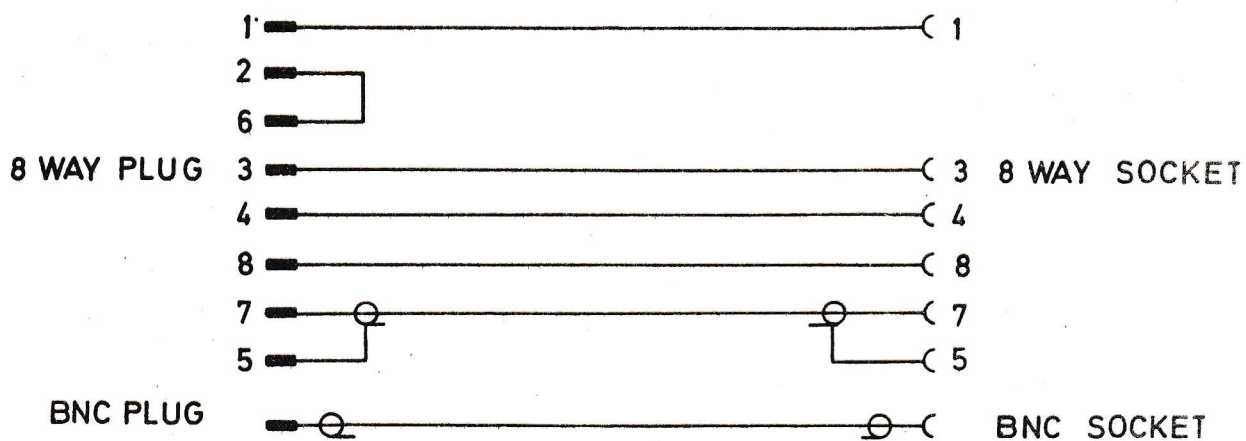
## APPENDIX C

### USING THE RECEIVER WITHOUT A CRYSTAL UNIT OR SYNCHRONISER

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#### SYNCHRONISER EXTENSION LEAD

The lead is required to operate the synchroniser out of the receiver. It should be approx. 800mm (31½") long.



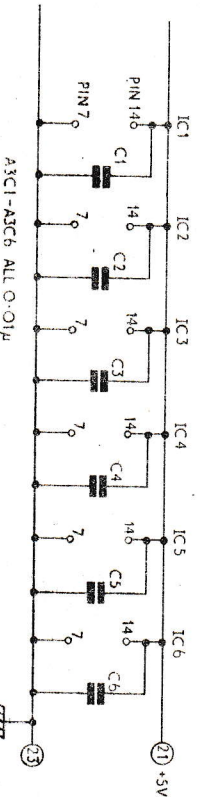
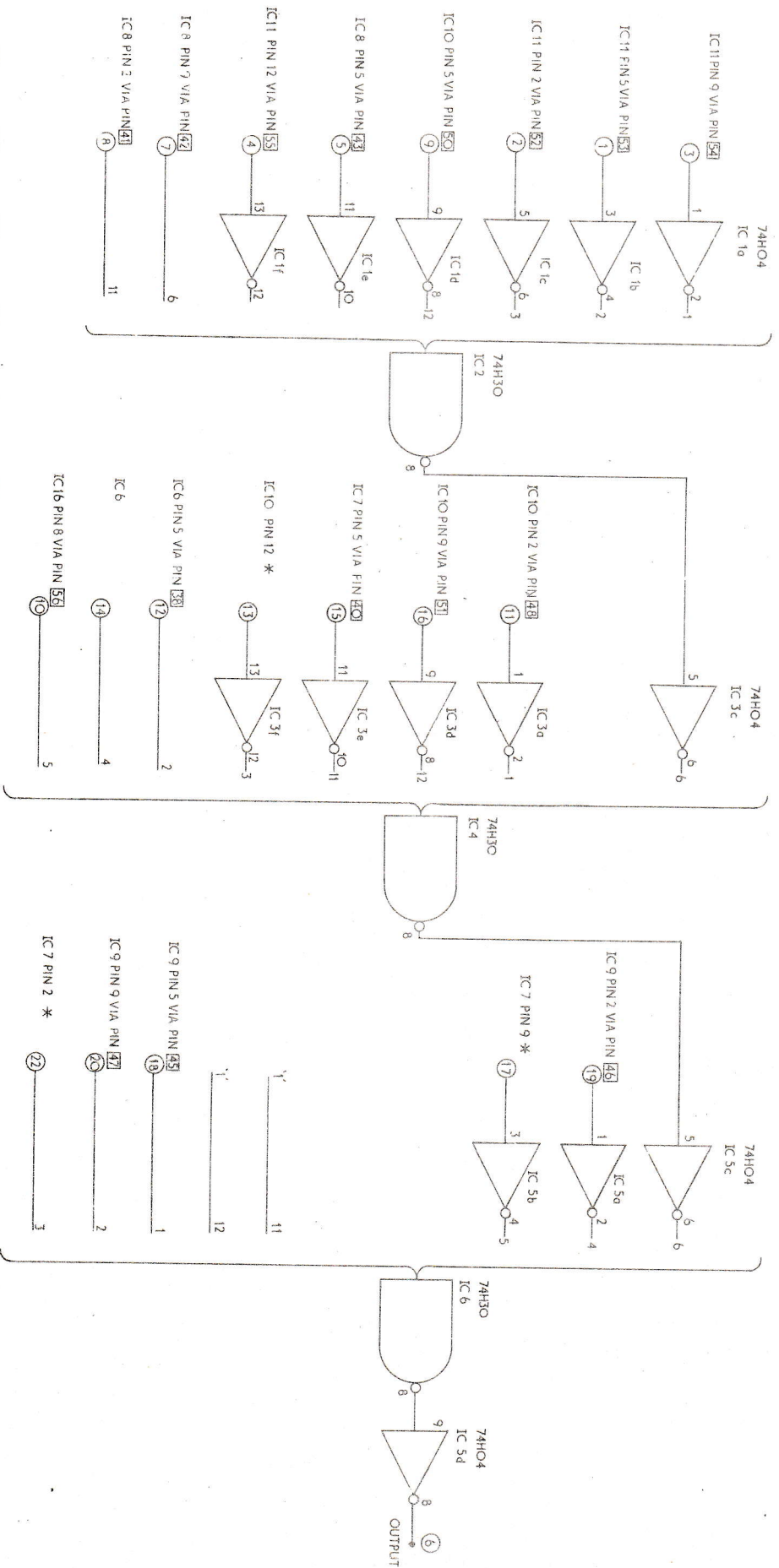


NOTE:-

CIRCUIT DIAGRAM BP1459

- (1) This sub-circuit replaces that circuitry shown on the main synchroniser diagram (area designation code A3) for the OFFSET BOARD on all synchronisers used in conjunction with the Eddystone Model 1990S Receiver.
- (2) The relevant PCB layout and legend illustrated at page B1 of this manual (Appendix B) relates solely to the above mentioned sub-circuit (BP1459).
- (3) Accordingly, the text and components list reflect the foregoing changes and relate solely to Model 1990S/Synchroniser operation.

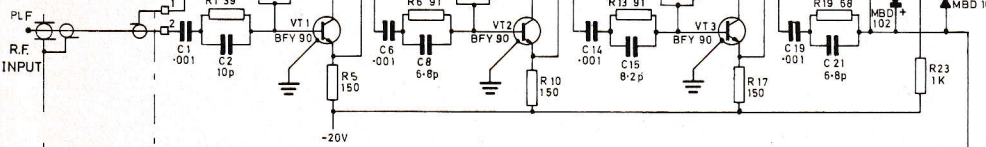
CIRCUIT REFERENCE PREFIX :: A3



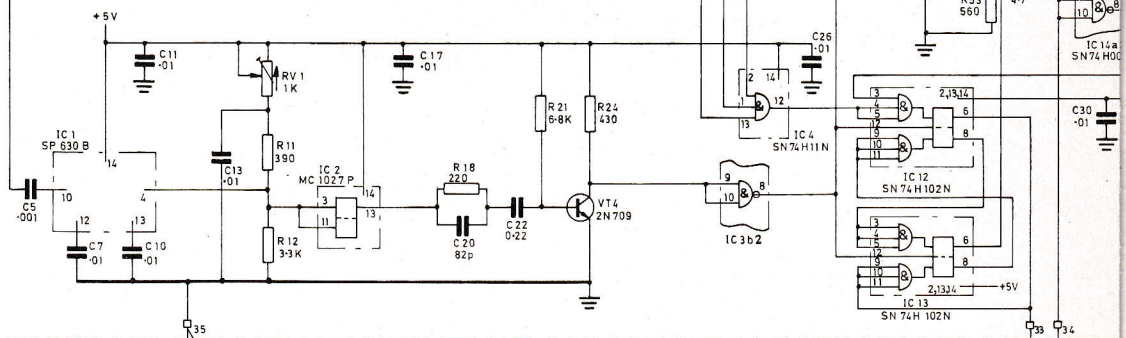
1990S SYNCHRONISER  
OFFSET BOARD

BP1459

# VARIABLE RATIO DIVIDER (A2) 44827-261L

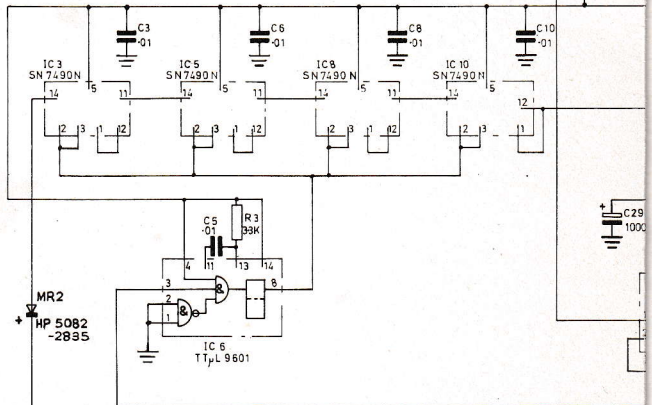


IC	PINS EARTHED IN ADDITION TO THOSE SHOWN ON CIRCUIT
1	7
2	4,5,6,7,8,9,10,12
3	7
4	7
5	7
6	7
7	7
8	7
9	7
10	7
11	7
12	7
13	7
14	7
15	7

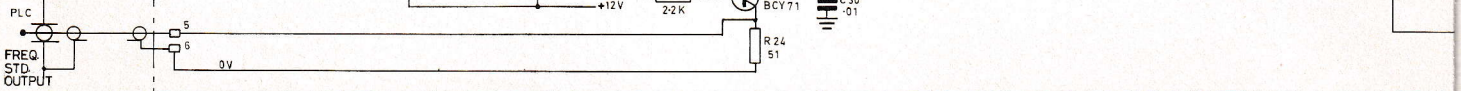


IC	PINS EARTHED IN ADDITION TO THOSE SHOWN ON CIRCUIT
1	2,3,6,7,10
2	2,3,6,7,10
3	6,7,10
4	2,3,6,7,10
5	6,7,10
6	7
7	2,3,6,7,10
8	6,7,10
9	2,3,6,7,10
10	6,7,10
11	7
12	7
13	7
14	7
15	7

## STANDARD DIVIDER (A5) 44827-315R

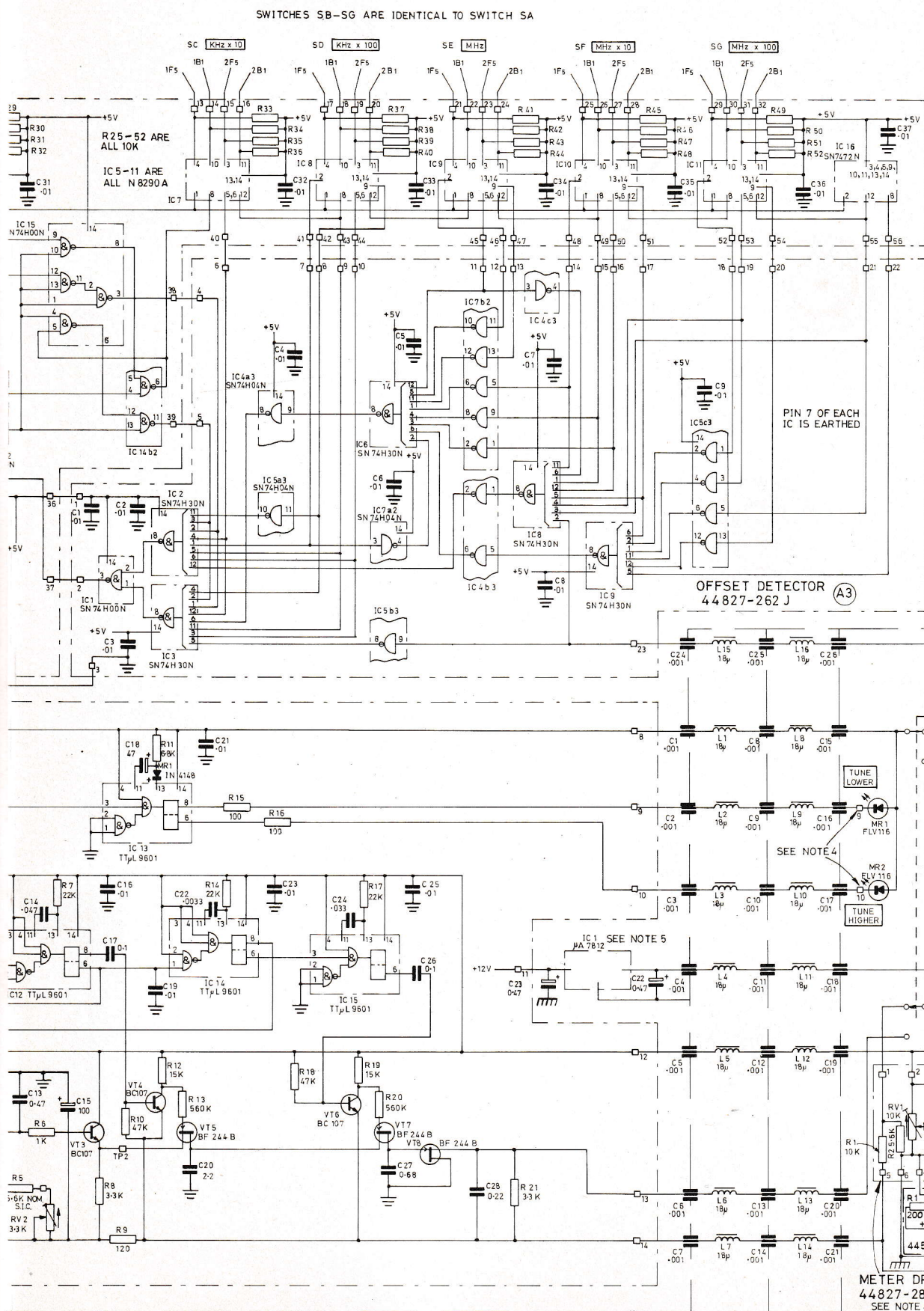


### 5MHz CRYSTAL OSCILLATOR



PLC  
FREQ.  
STD.  
OUTPUT





1. PRINTED BOARD PERIMETER

2. RF SCREENING

3. COMPONENTS NOT ON PRINTED BOARDS ARE IN A1.

4. TAGS 9 & 10, BETWEEN A1MR1 & A1C16 & BETWEEN A1MR2 & A1C17 RESPECTIVELY, ARE SITUATED ON METER DRIVE BOARD A4.

5. VOLTAGE REGULATOR CONNECTIONS:-

